

QMLE4/5

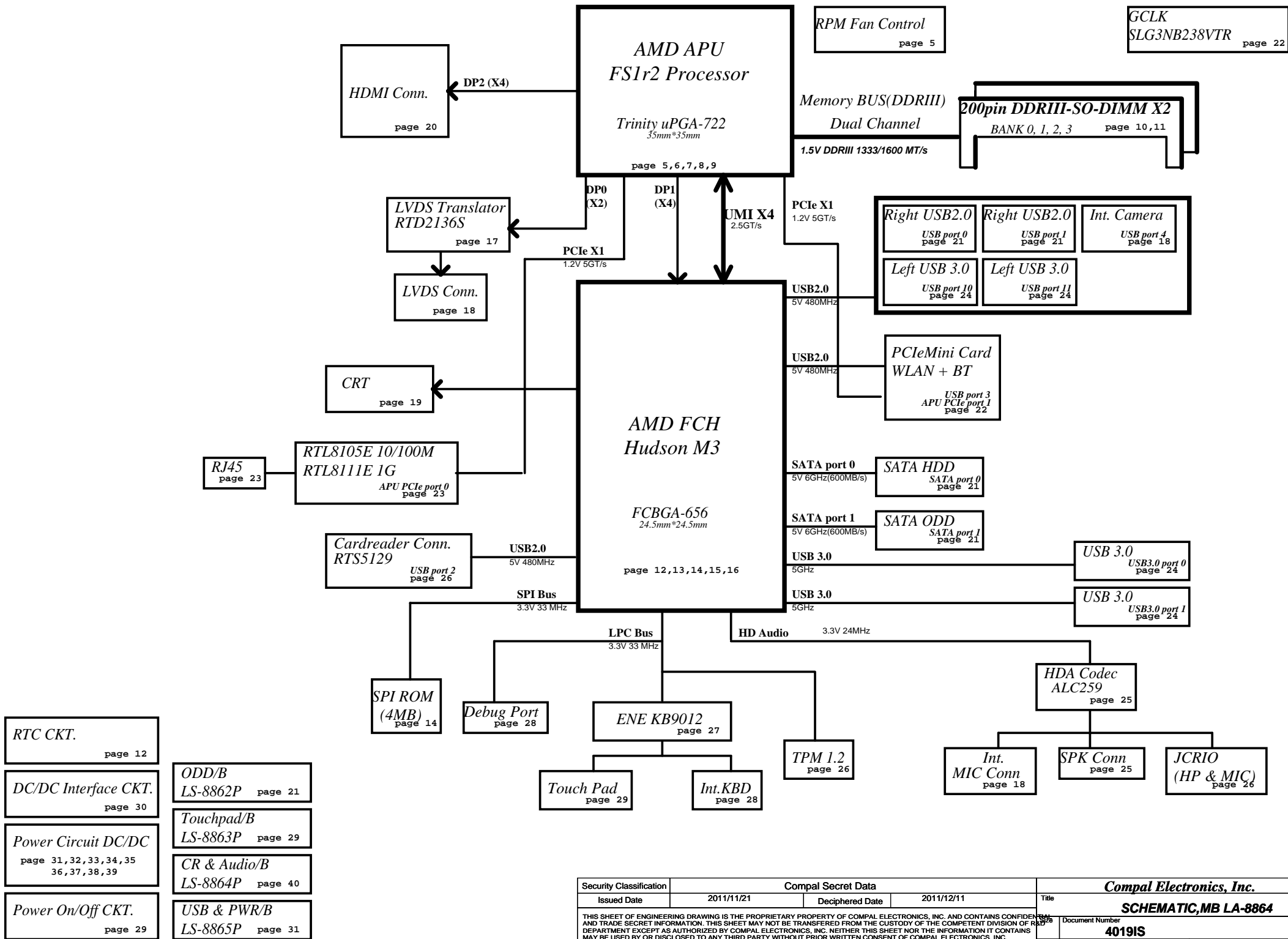
Eureka UMA

LA-8864P REV 0.3 Schematic

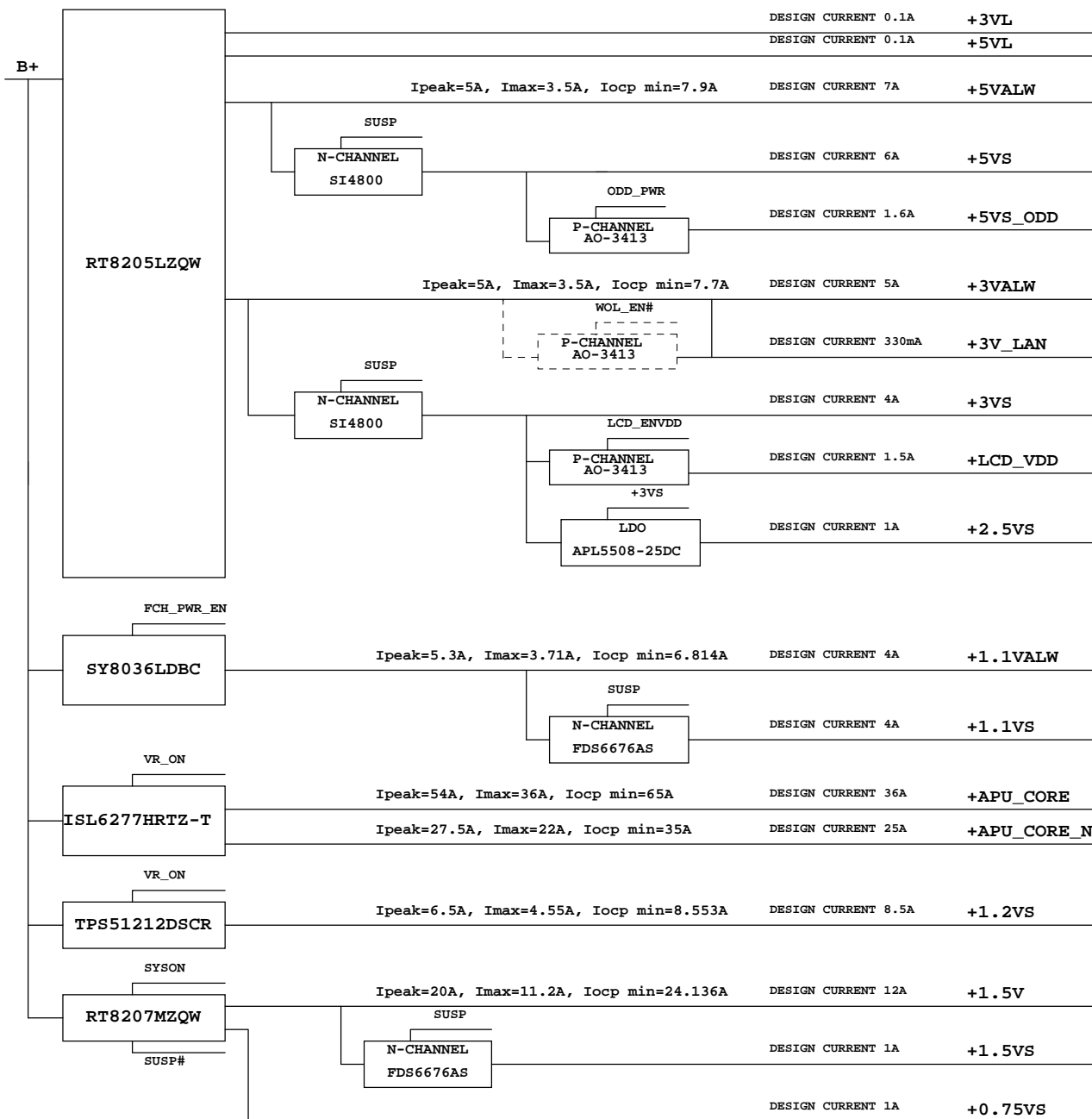
AMD Trinity FS1r2 APU / Hudson M3 FCH

2012-03-14 Rev 0.3

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size B	Document Number
				4019IS	
Date: Monday, March 26, 2012				Sheet 1	of 40



Security Classification		Compal Secret Data		Title	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev A
				4019IS	
Date: Monday, March 26, 2012		Sheet 2		of 40	



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019IS
				Date	Monday, March 26, 2012
				Sheet	3 of 40

Voltage Rails

(O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	FCH			Clock	
description	Hudson-M3			Clock	
explain	R1	R3	UNBW	Green Clock	No Green Clock
BTO	HUDM3R1@	HUDM3R3@	HUDM3UNBW@	GCLK@	NOGCLK@

Function	LAN		Camera	Internal Analog MIC	TPM	
description	LAN		Camera	Internal Analog MIC	TPM	
explain	10/100M	GIGA	Camera	Internal Analog MIC	9635	9655
BTO	8105ELDO@	8111FVB@	CAM@	AMIC@	TPM9635@	TPM9655@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

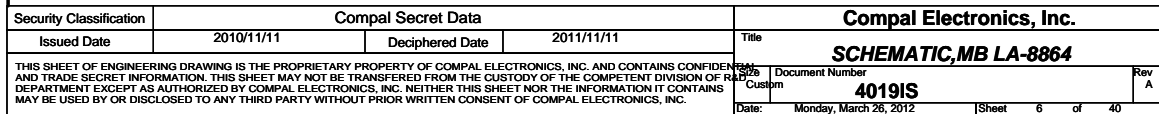
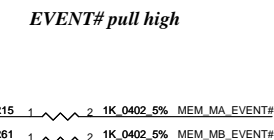
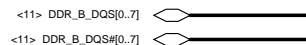
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b
EC SM Bus2 Address			
Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b

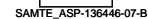
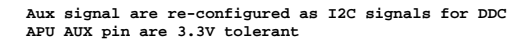
EC SM Bus3 Address

Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

<div>SIGNAL</div> <div>STATE</div>	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/11/21		Deciphered Date		2011/12/11		Title	
								SCHEMATIC, MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.									
						Document Number		Rev	
						4019IS		A	
						Date: Monday, March 26, 2012		Sheet 4 of 40	





temperature:

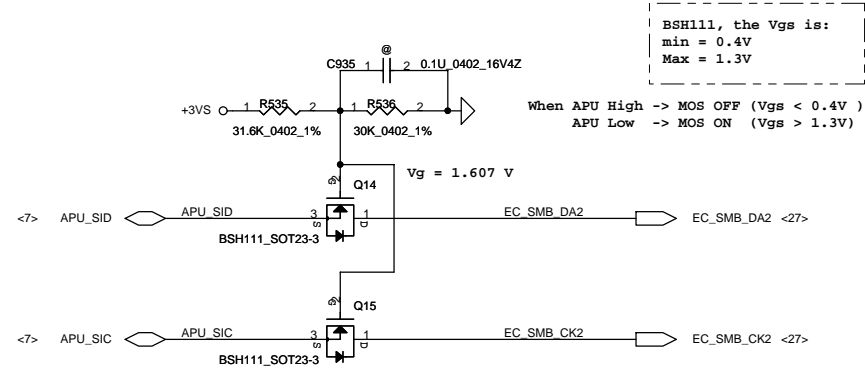
APU_THERMTRIP#

MMBT3904, NLT, SOT23-3

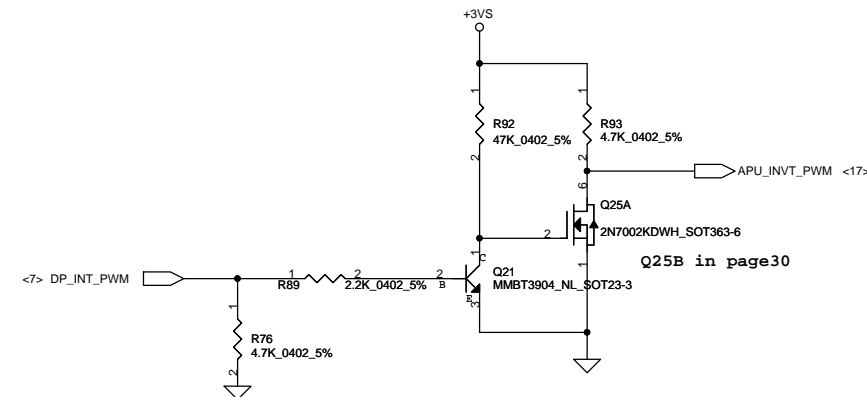
H_THERMTRIP# <13>

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	4019IS
				Document Number	Rev A
Date:	Monday, March 26, 2012	Sheet	7	of	40

SB-TSI

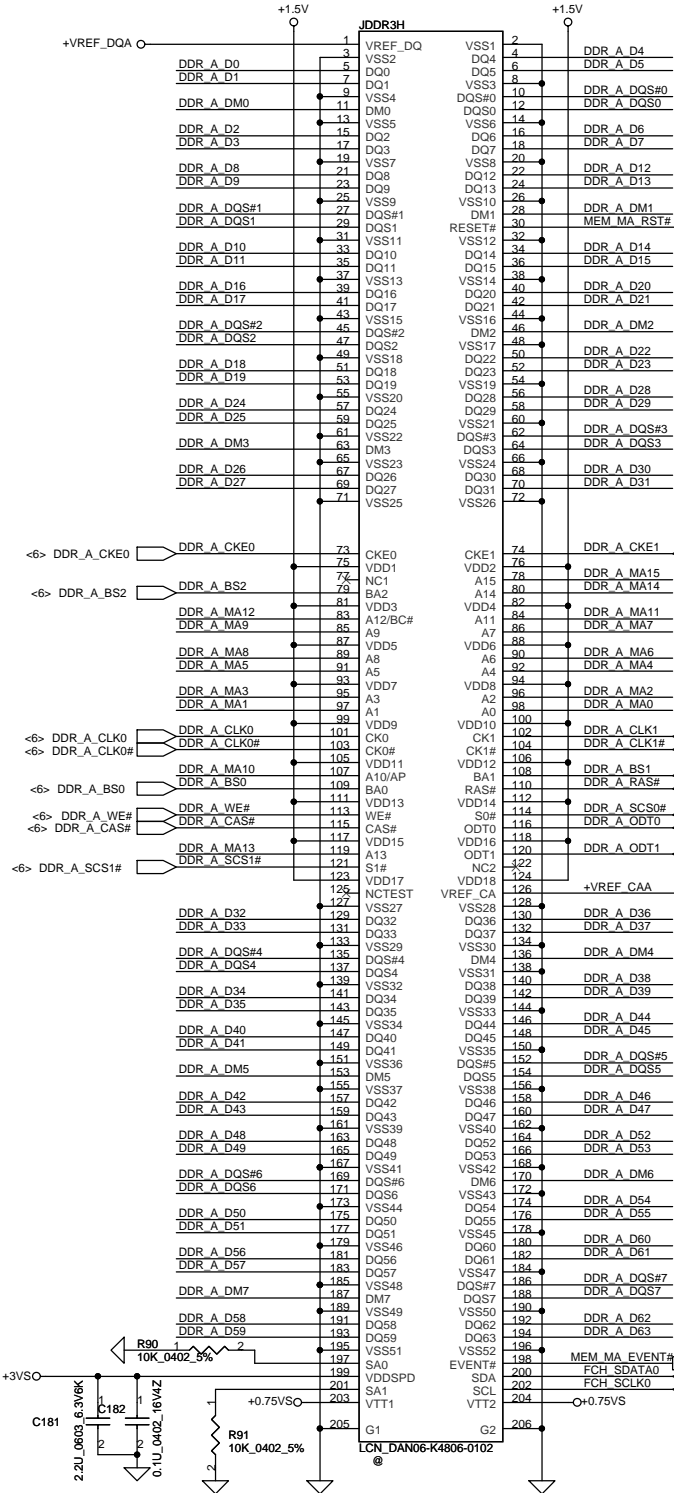


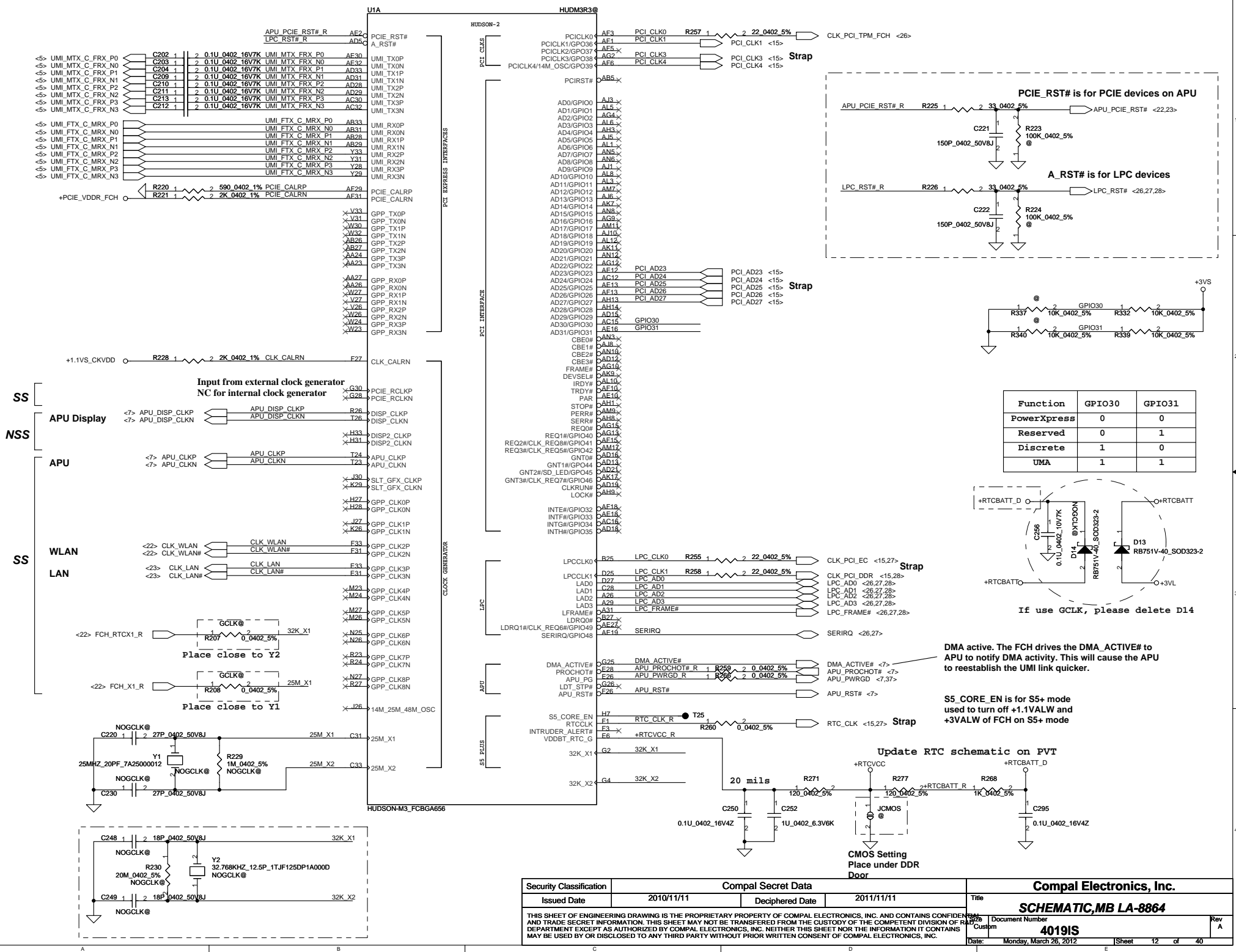
Panel PWM



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC,MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019IS
				Date	Monday, March 26, 2012
				Sheet	9 of 40
				Rev	A

DDR3 SO-DIMM A Standard Type





SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

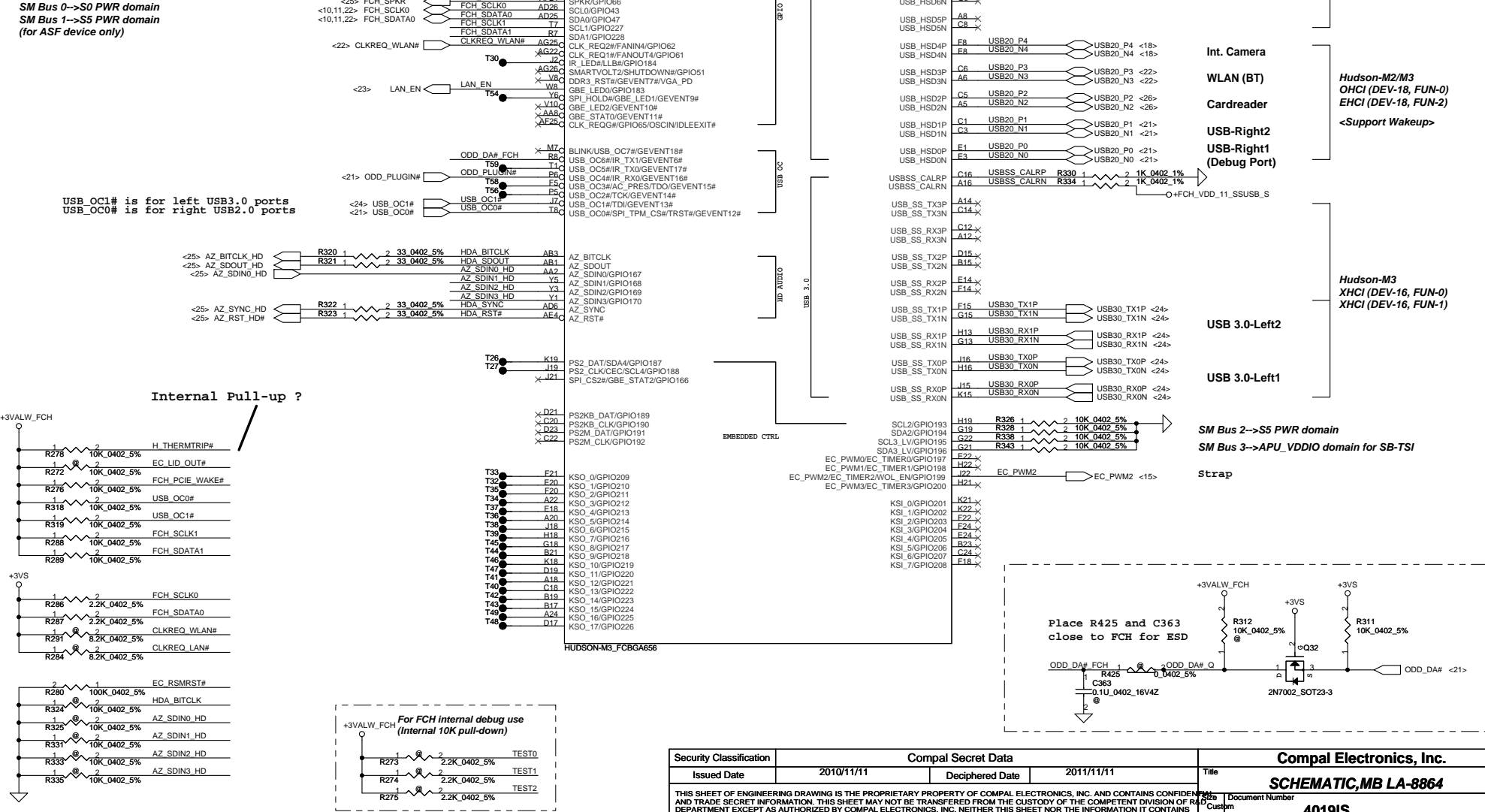
USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports

Internal Pull-up ?

PCIE_RST2# is for PCIE devices on FCH

U10

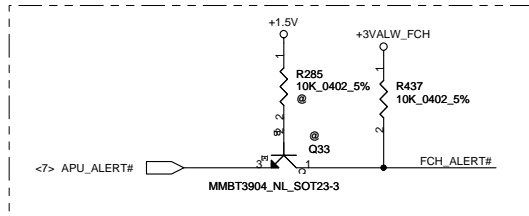
HUDM3R3@



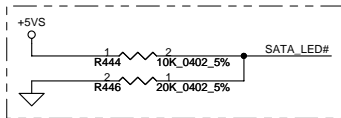
HDD

14" ODD

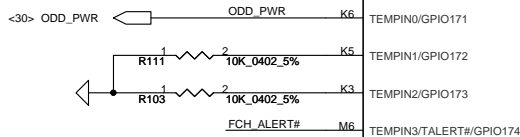
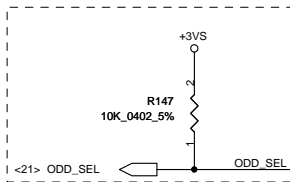
15"/17" ODD



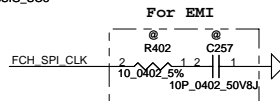
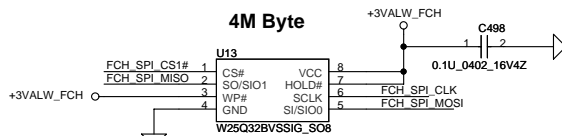
To avoid LED flashing



ODD_SEL	SATA port	SKU
High	Port 1	14 "
Low	Port 2	15"/17"



4M Byte



U1B

HUDSON-2

HUDM3R3@

SERIAL ATA

HW MONITOR

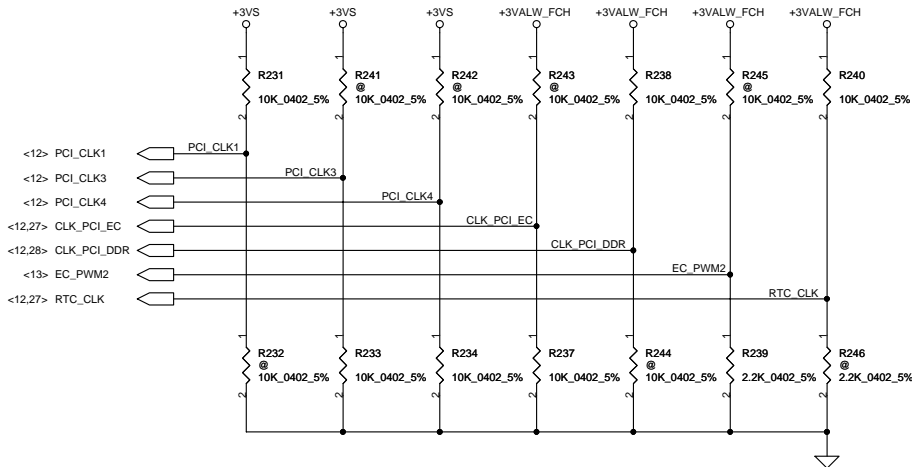
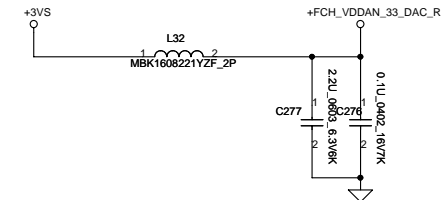
HUDSON-M3_FCBGA656

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/11/11	Deciphered Date	2011/11/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Document Number 4019IS
Date: Monday, March 26, 2012					Sheet 14 of 40

STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

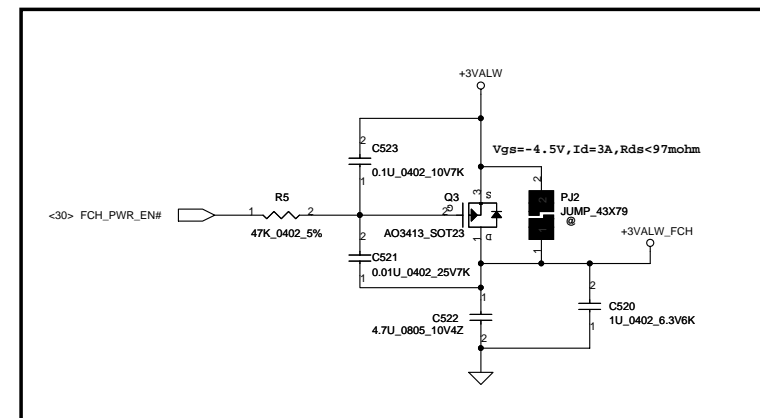
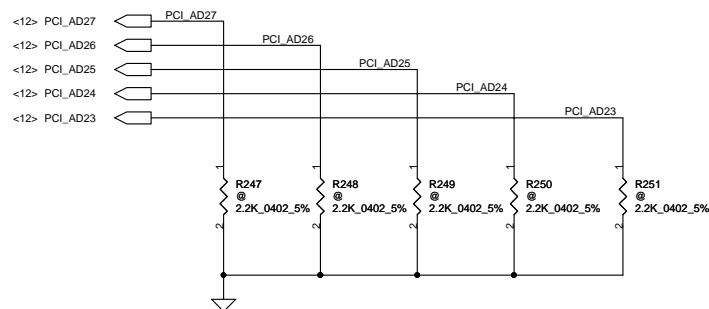
CRT Power Down Circuit



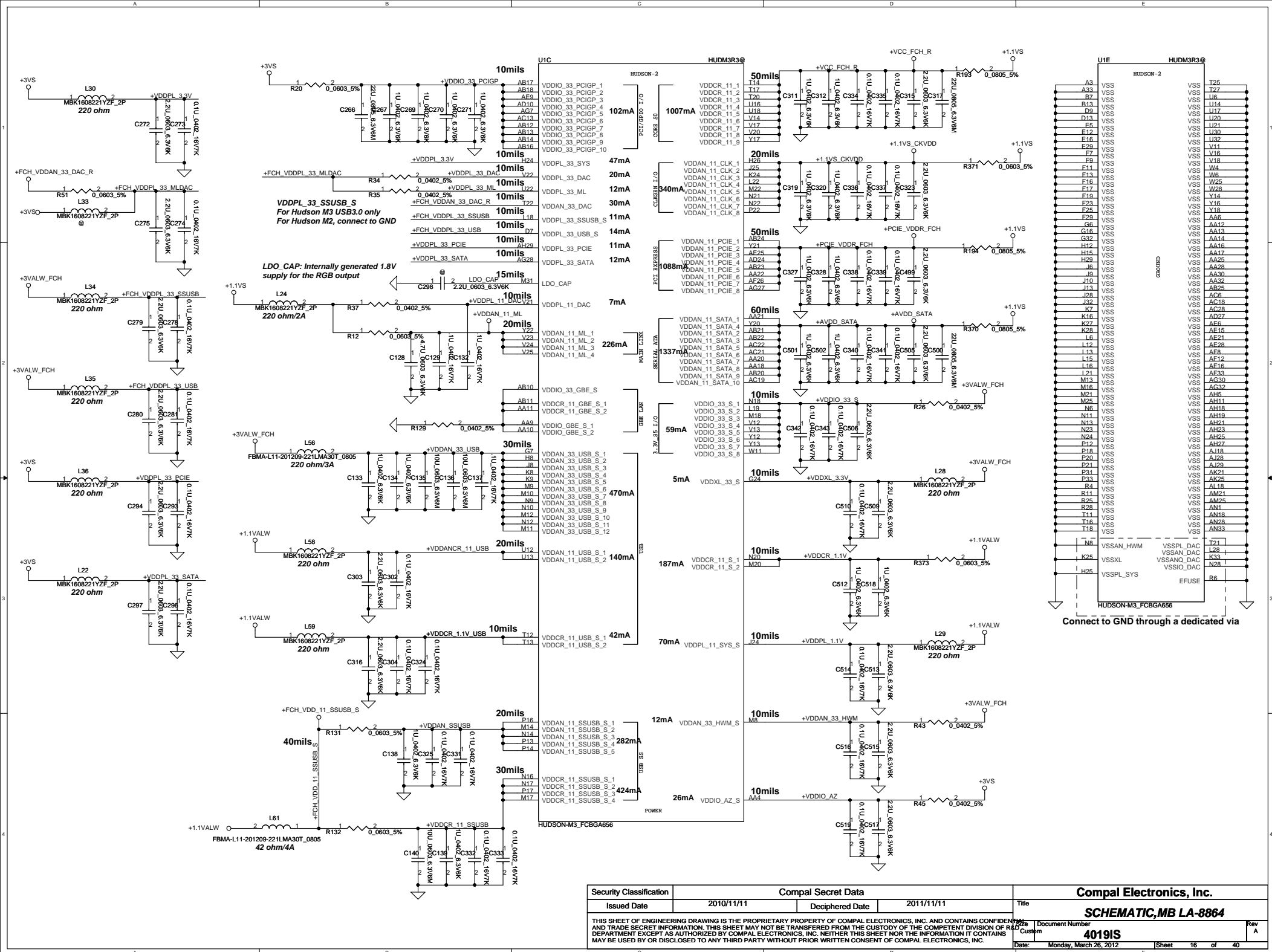
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/11/11	Deciphered Date	2011/11/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019IS
				Date	Monday, March 26, 2012
				Rev	A
				Sheet	15 of 40

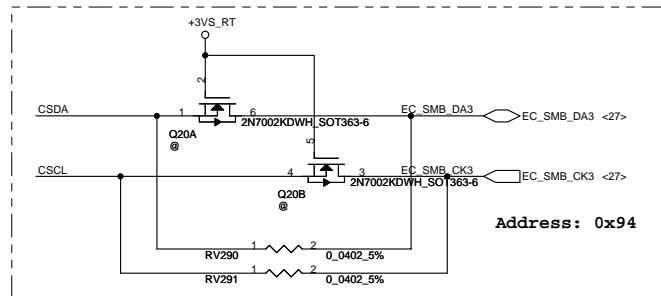
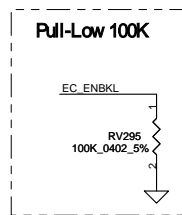
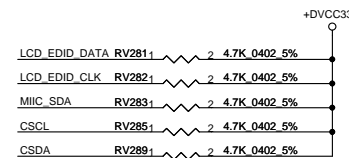
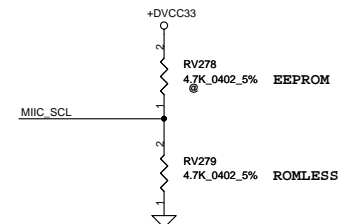
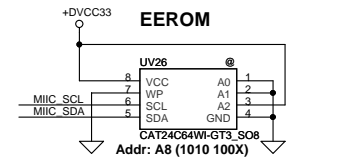
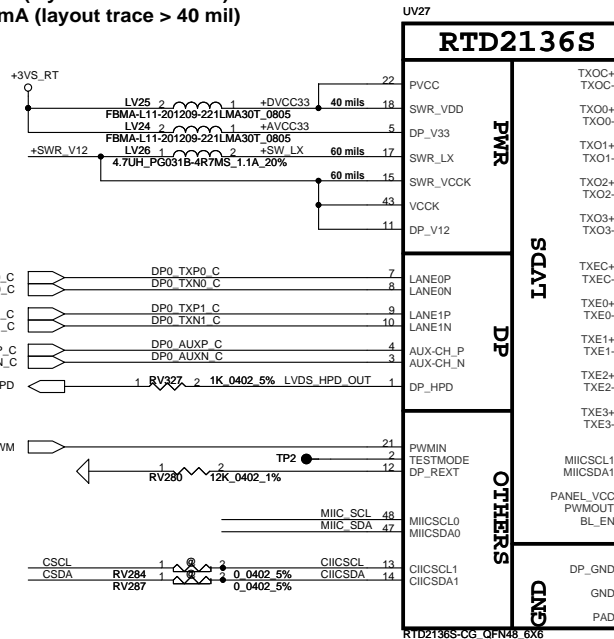
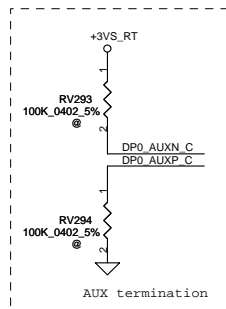
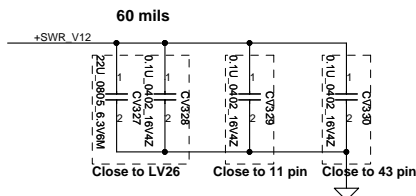
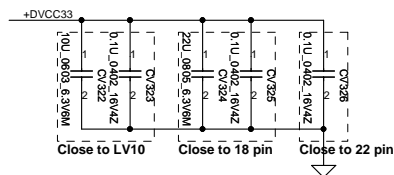
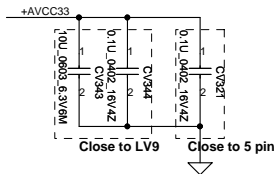


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/11/11	Deciphered Date	2011/11/11	Title	SCHEMATIC, MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	Document Number	Rev
				Custom	4019IS	A
				Date:	Monday, March 26, 2012	Sheet 16 of 40

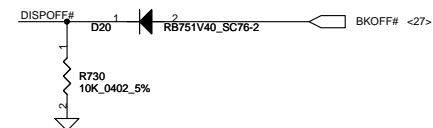
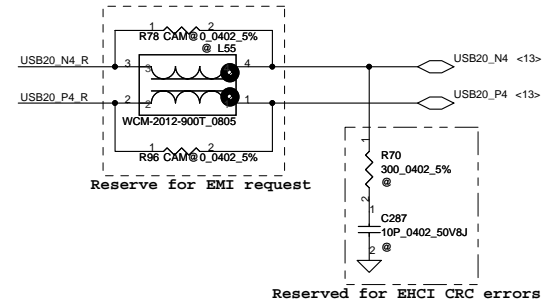
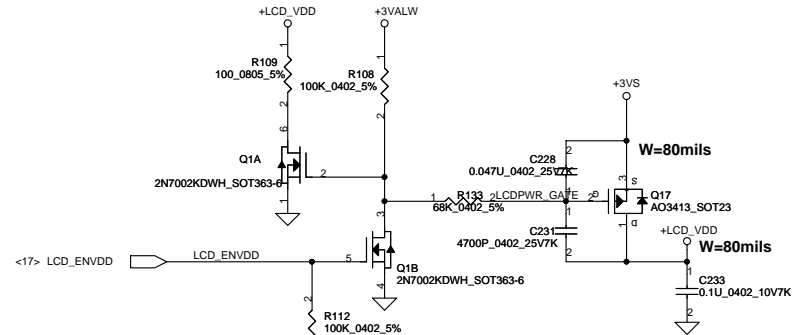
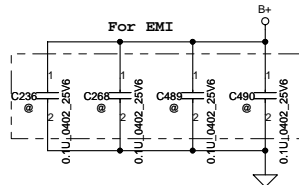
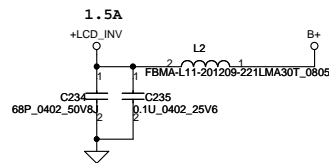
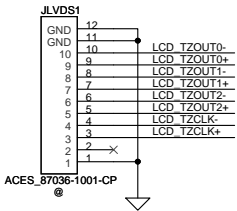
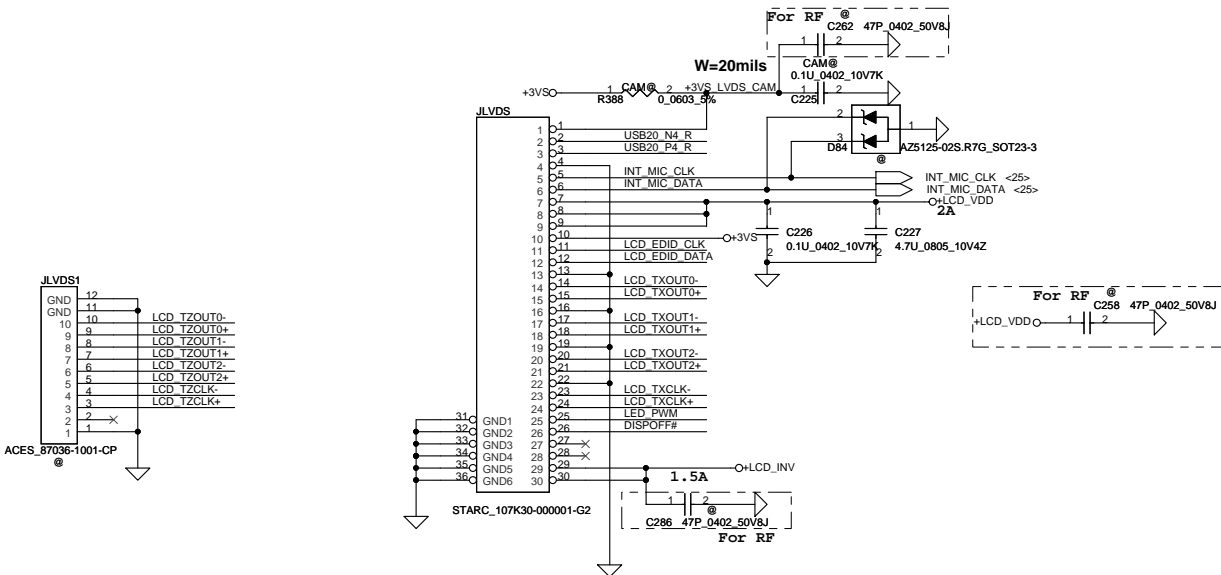
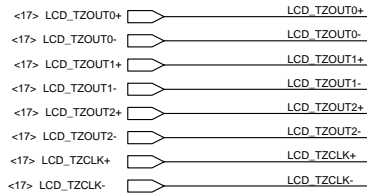
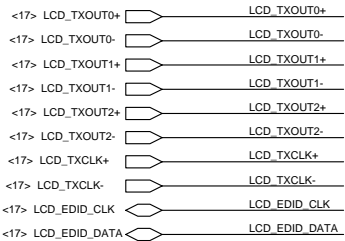


Power Consumption:

Pin5 (DPV33) < 20mA
 Pin 11 (DPV12) < 100mA
 Pin 15 (SWR_VCCCK) < 100mA (layout trace > 60 mil)
 Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 22 (PVCC) < 50 mA
 Pin 43 (VCCCK) < 50mA

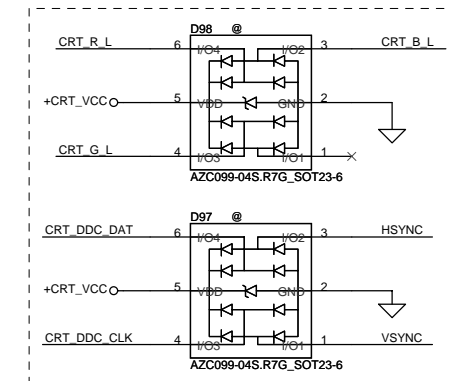
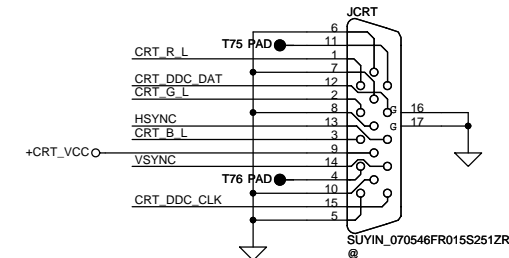
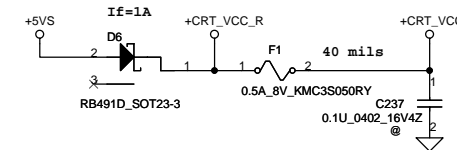
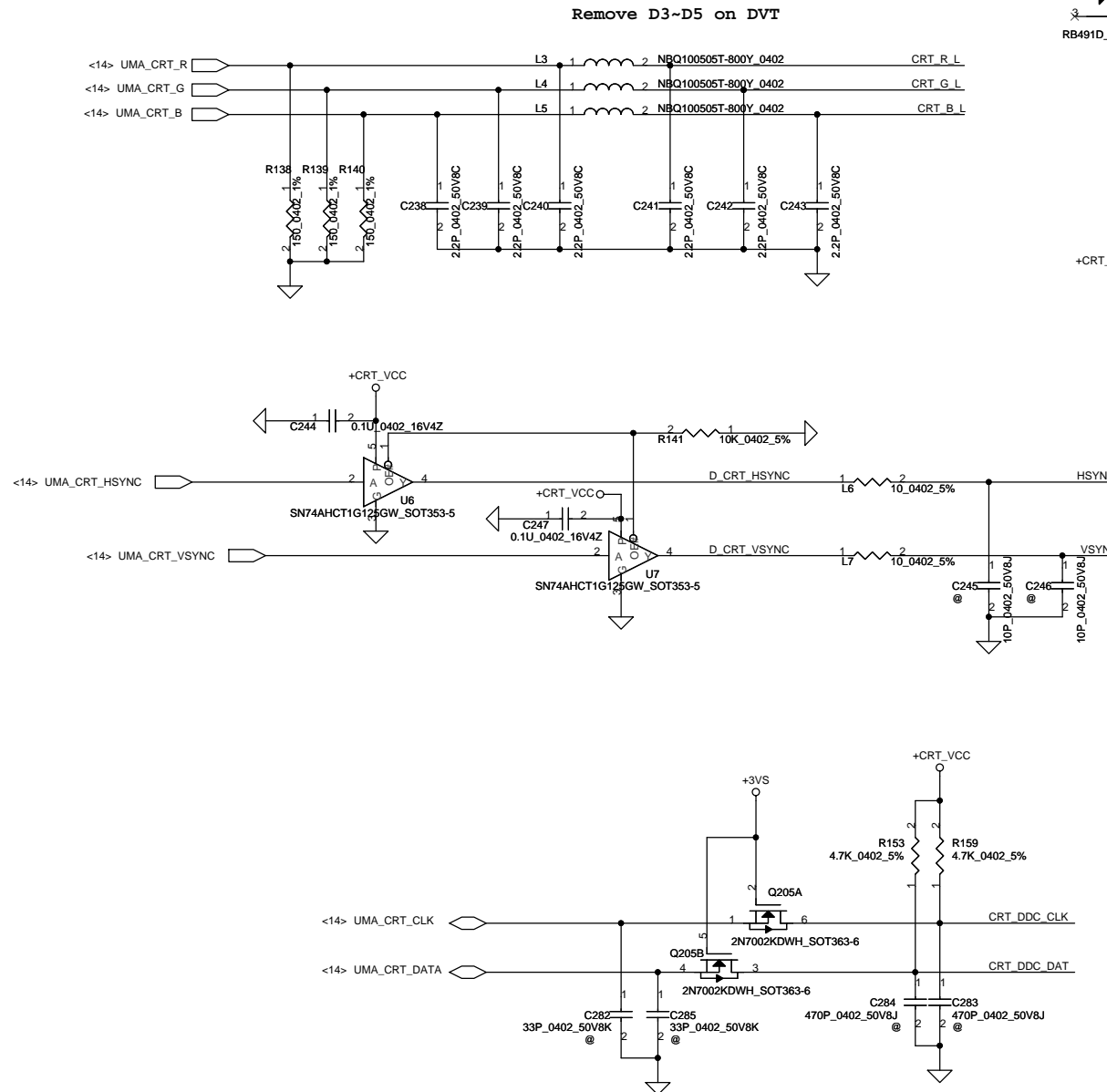


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/11/11				Title			
Deciphered Date				2012/12/31				SCHEMATIC, MB LA-8864			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date				Monday, March 26, 2012			
				Document Number				4019IS			
				Rev				A			
				Sheet				17 of 40			



Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2011/11/11		Deciphered Date		2012/12/31		Title							
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								SCHEMATIC, MB LA-8864							
								Rev A		Document Number		4019IS		Rev A	
								Date: Monday, March 26, 2012		Sheet		18		of 40	

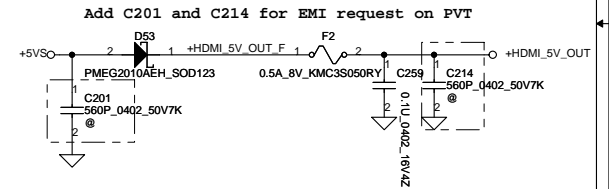
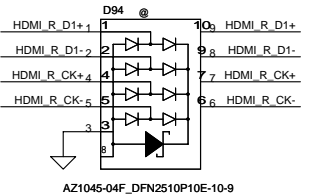
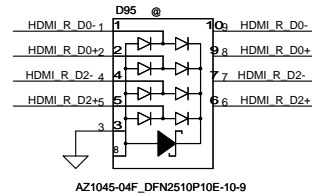
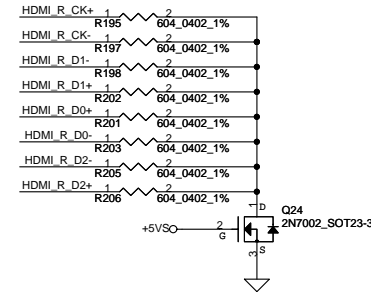
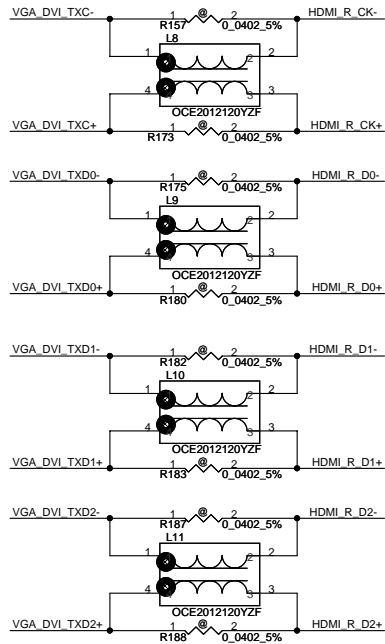
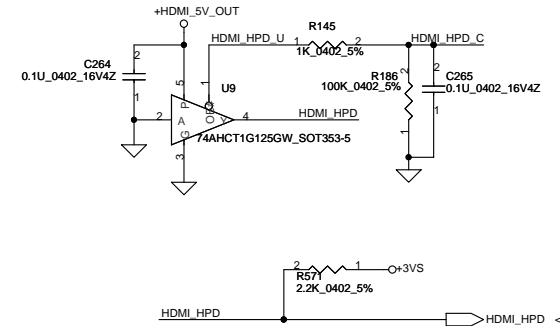
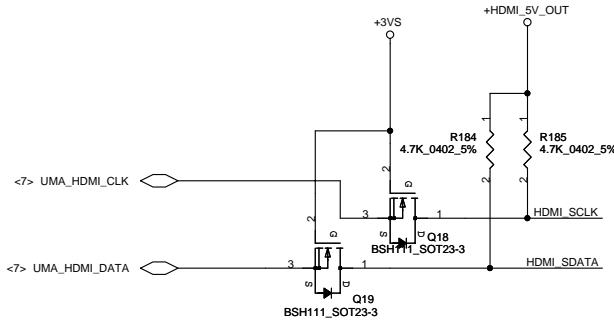
CRT CONNECTOR



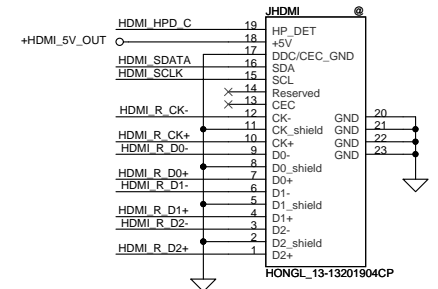
Reserve ESD for CRT connector on DVT

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019IS
				Date	Monday, March 26, 2012
				Sheet	19 of 40

<7> UMA_HDMI_TXC+	CV308	1	2	0.1U_0402_16V7K	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	CV304	1	2	0.1U_0402_16V7K	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	CV306	1	2	0.1U_0402_16V7K	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	CV302	1	2	0.1U_0402_16V7K	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	CV303	1	2	0.1U_0402_16V7K	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	CV301	1	2	0.1U_0402_16V7K	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	CV307	1	2	0.1U_0402_16V7K	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	CV305	1	2	0.1U_0402_16V7K	VGA_DVI_TXD2-



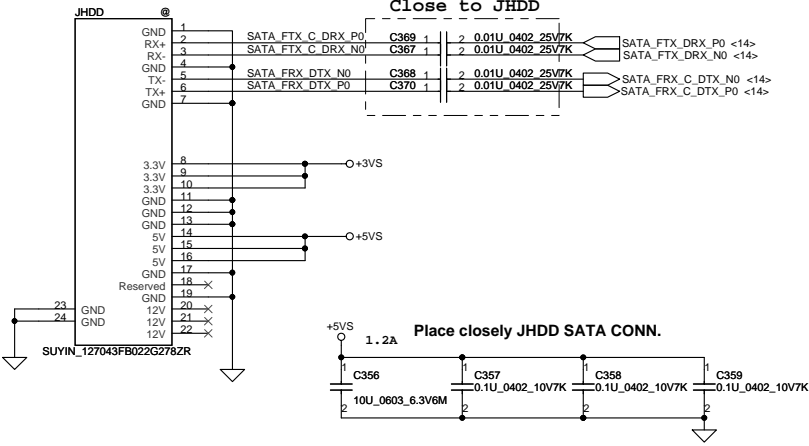
HDMI Connector



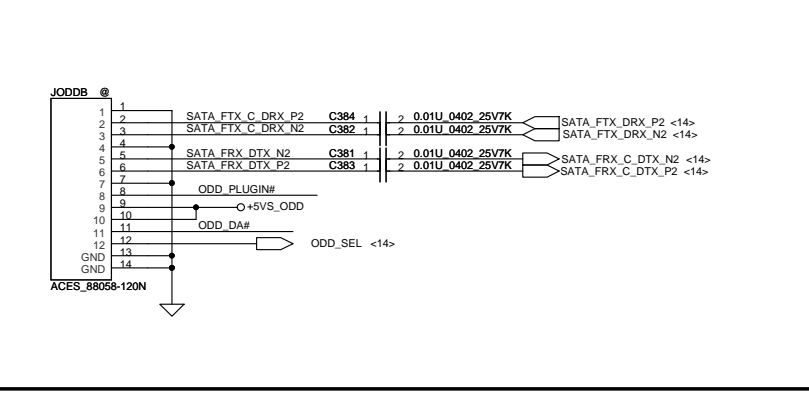
Reserve ESD for HDMI conn. on DVT

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Document Number
					4019IS
					Rev A
					Date: Monday, March 26, 2012
					Sheet 20 of 40

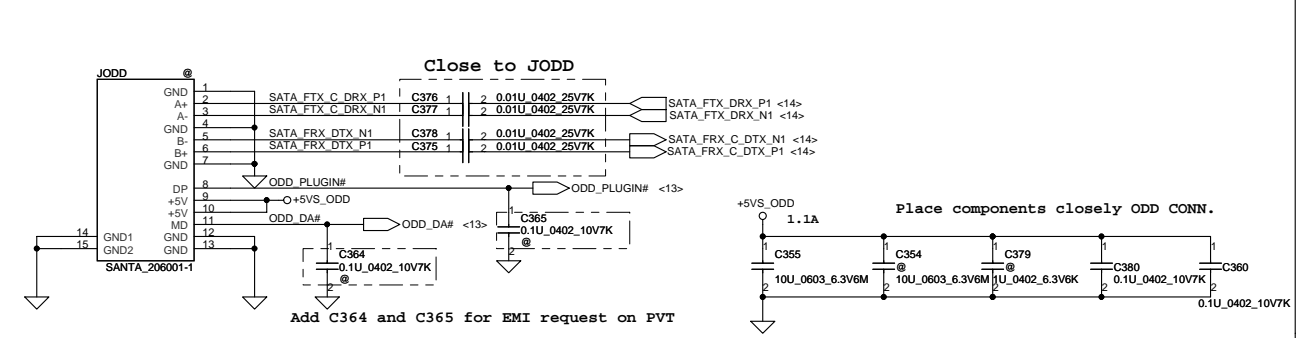
SATA HDD Conn.



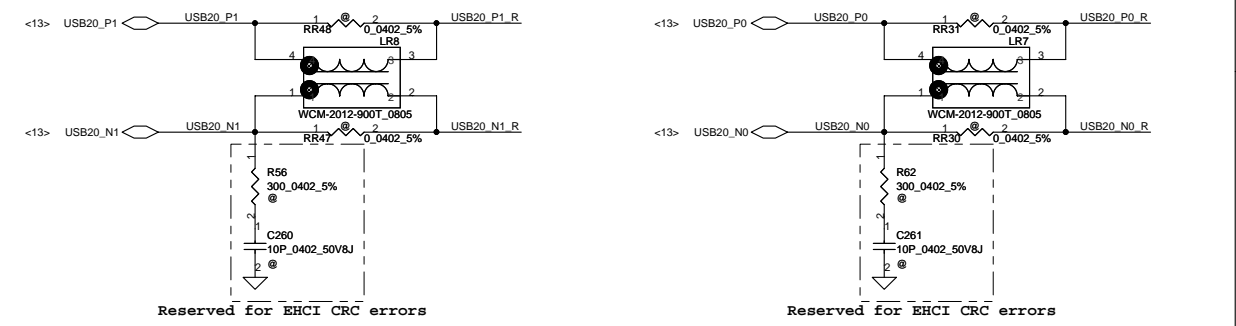
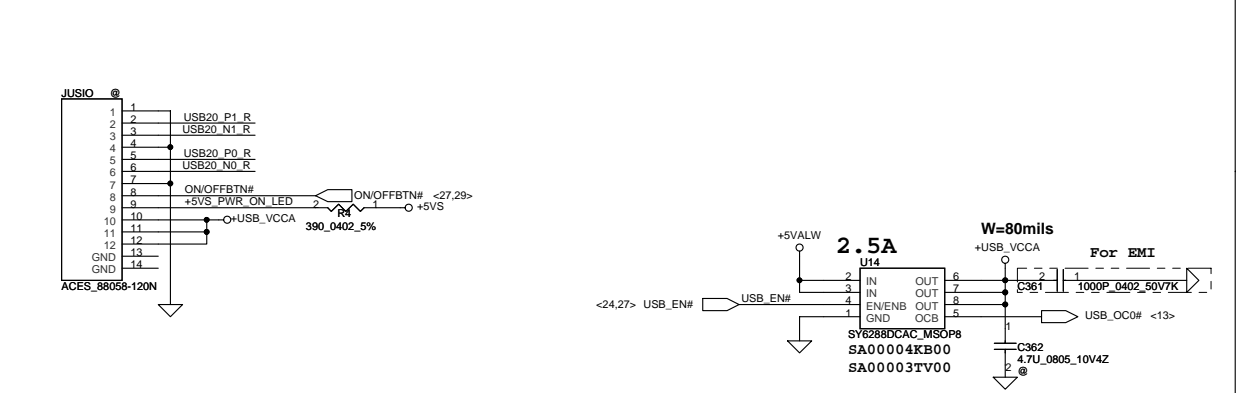
SATA ODD Conn (for 15"/17")



SATA ODD Conn (for 14")



Power Button & RUSB connector



Security Classification		Compal Secret Data		Title	
Issued Date	2011/11/11	Deciphered Date	2012/12/31	SCHEMATIC,MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev A
				4019IS	
				Monday, March 26, 2012	Sheet 21 of 40

40 mils

For SED

1.5V5_WLAN

U 0402_16V4Z

CM2

CM3

47P_0402_50V8J

C253

U7K

4.7U_0805_10V4Z

For SED

U 0402_16V4Z

CM7

CM8

CM9

47P_0402_50V8J

C254

0.01U_0402_25V7K

4.7U_0805_10V4Z

+1.5V5_WLAN

PJ33

PAD-OPEN 2x2m

+1.5V5_WLAN

+3V_WLAN

BT_ON

R1443

0_0402_5%

2BT_CTRL R

<13> CLKREQ_WLAN#

<12> CLK_WLAN#

<12> CLK_WLAN

<5> PCIE_FRX_WLANTX_N1

<5> PCIE_FRX_WLANTX_P1

<5> PCIE_FTX_C_WLANRX_N1

<5> PCIE_FTX_C_WLANRX_P1

WLAN/ WIFI

+3V_WLAN_O

R17

0_0402_5%

E51_TXD

E51_TXD_R

E51_RXD

E51_RXD_R

Debug card using

R49

0_0402_5%

JWLAN

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

G1

G2

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

BELLW_80003-7041

R47

0_0402_5%

WLAN_OFF# 1

WLAN_RST# R

WL_OFF#

<27>

FCH_SCLK0 <10,11,13>

FCH_SDAT0A0 <10,11,13>

USB20_N3 <13>

USB20_P3 <13>

BT

R63


300_0402_5%

C263

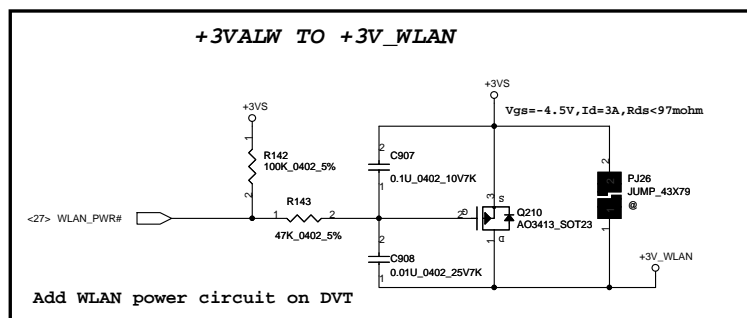
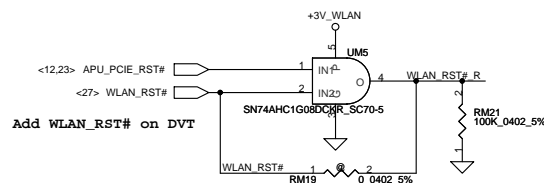
10P_0402_50V8J

Change JWLAN symbol to SP07000TB00 on DVT

Reserved for EHCI CRC errors

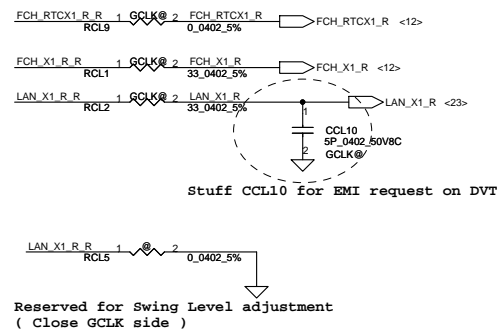
<27> BT_ON  1 R327 2 E51 RXD R
 1K 0402 5%

For isolate BT_CTRL and Compal Debug Card.

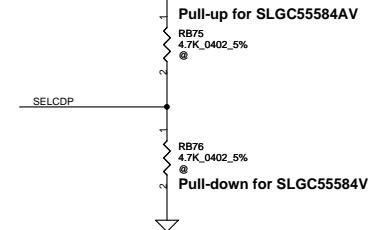
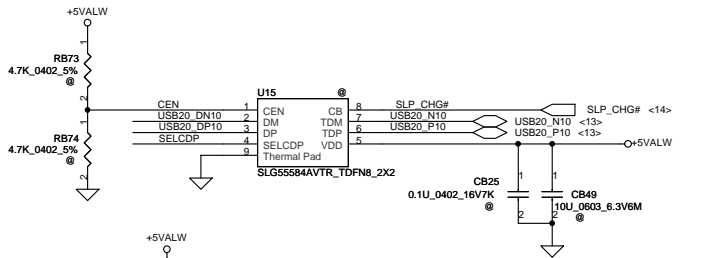


The schematic diagram illustrates the Green Clock Generator circuit. It features a central UCL1 (SLG3NB238VTR) IC, which is a 16P_2X3 device. The IC is connected to various power and signal pins:

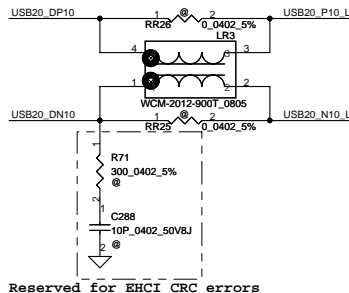
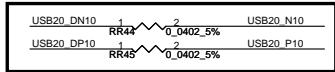
- Power Pins:**
 - +3VALW** and **+3VLO** are connected to pin 2 (VDD +V3.3A).
 - +3V_LAN** and **+3VS** are connected to pin 8 (VDDIO_25M_A) and pin 3 (VDDIO_25M_B).
 - +3V_LAN** and **+3VS** are also connected to pin 1 (CLK_X1) and pin 16 (CLK_X2).
 - +3V_LAN** and **+3VS** are connected to pin 4 (VSS), pin 7 (VSS), pin 13 (VSS), and pin 17 (Thermal Pad).
- Signal Pins:**
 - CLK_X1** and **CLK_X2** are connected to pin 1 (CLK_X1) and pin 16 (CLK_X2).
 - XTAL_OUT** and **XTAL_IN** are connected to pin 1 (CLK_X1) and pin 16 (CLK_X2).
 - VDD_RTC_OUT** is connected to pin 14.
- Capacitors:**
 - CCL8** (0.1u_0402_107K) is connected to pin 2 (VDD +V3.3A).
 - CCL1** (0.1u_0402_107K) is connected to pin 8 (VDDIO_25M_A).
 - CCL2** (0.1u_0402_107K) is connected to pin 1 (CLK_X1).
 - CCL3** (0.1u_0402_107K) is connected to pin 16 (CLK_X2).
 - CCL4** (18P_0402_50V8J) is connected to pin 2 (GND).
 - CCL5** (18P_0402_50V8J) is connected to pin 3 (GND).
 - CCL6** (2.2u_0603_6.3V6K) is connected to pin 14 (VDD_RTC_OUT).
 - CCL7** (2.2u_0805_6.3V6M) is connected to pin 10 (VBAT NC).
- Other Connections:**
 - RTC_BATT** is connected to pin 11 (NC).
 - RTC_BATT_D** is connected to pin 14 (VDD_RTC_OUT).
 - FCH_RTCX1_R_R** is connected to pin 9 (32K NC).
 - FCH_X1_R_R** and **LAN_X1_R_R** are connected to pin 5 (25M_B) and pin 6 (25M_A).



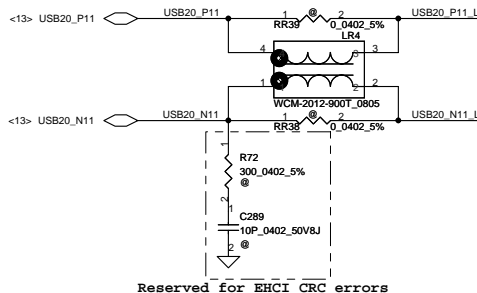
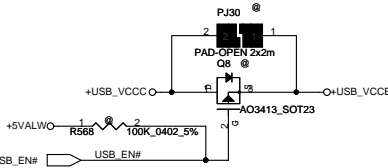
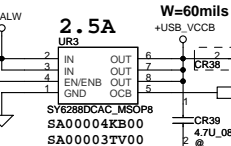
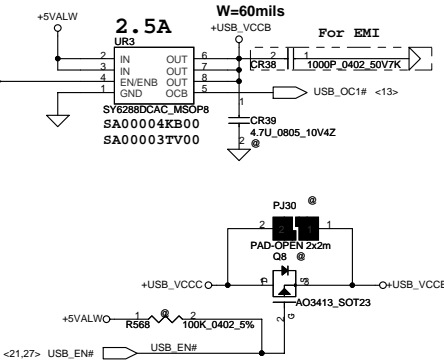
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/11/11	Deciphered Date	2011/11/11	Title	SCHEMATIC, MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					4019IS	A
Date:				Monday, March 26, 2012	Sheet	22 of 40



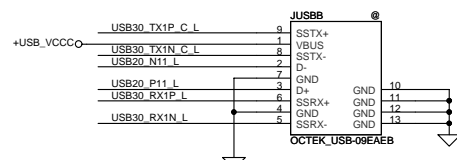
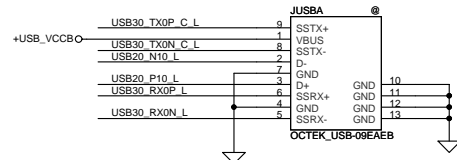
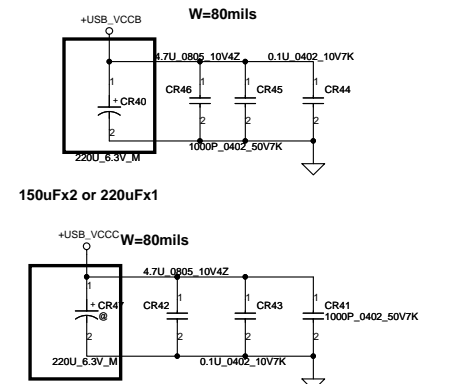
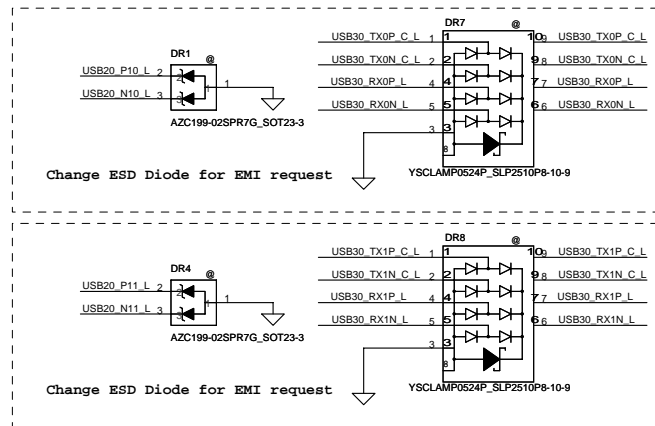
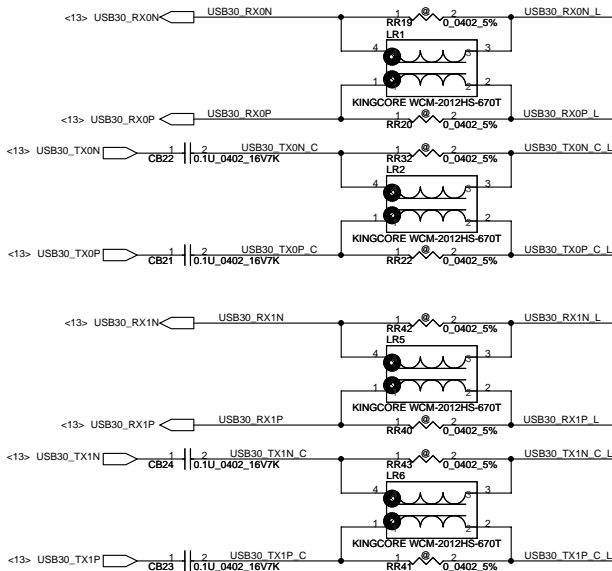
SLP_CHG#	SELCDP	Function
0	X	DCP autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only



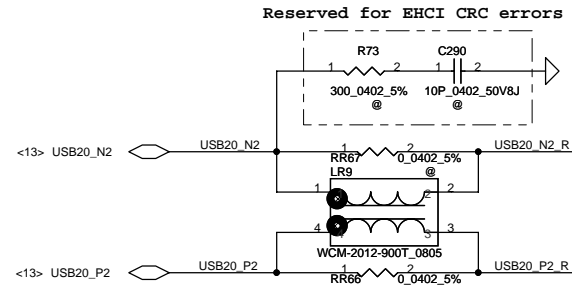
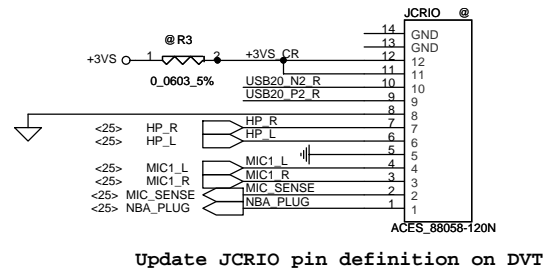
Reserved for EHCI CRC errors



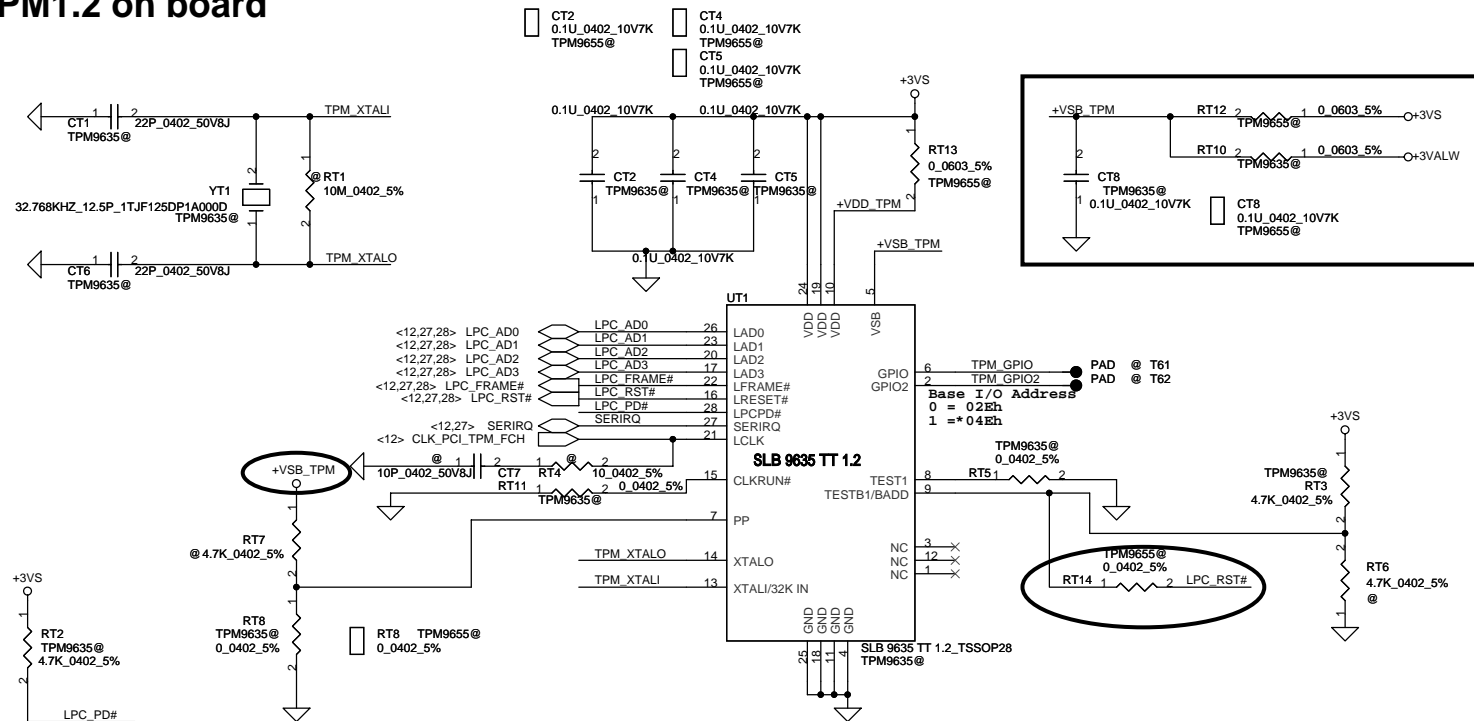
Reserved for EHCI CRC errors



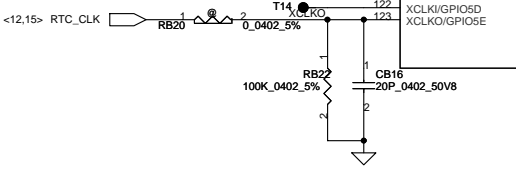
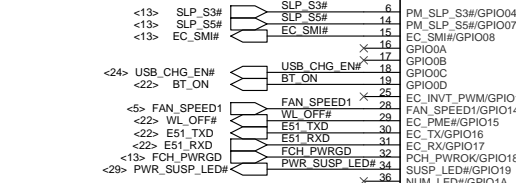
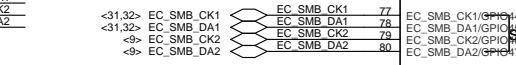
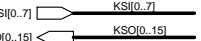
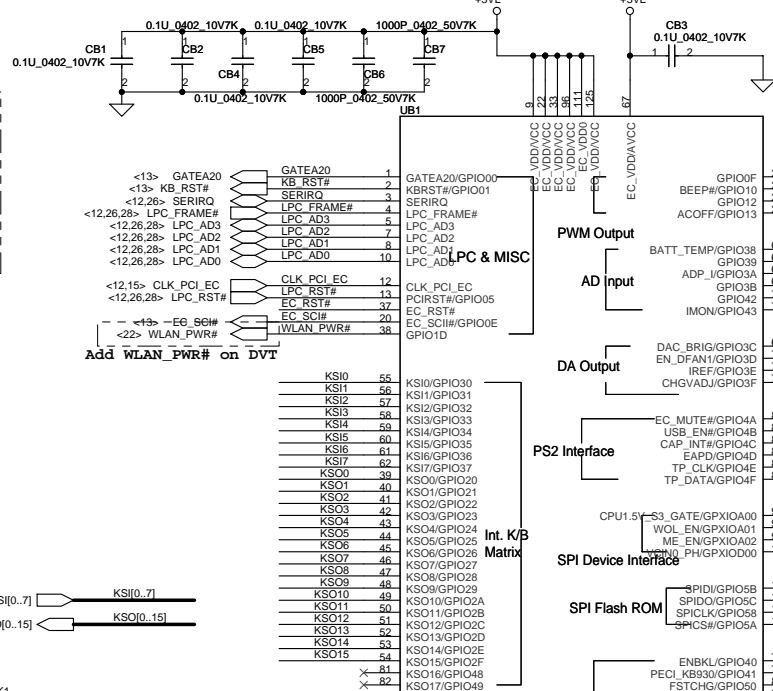
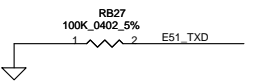
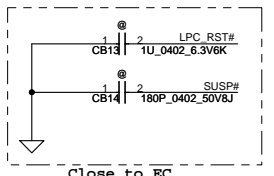
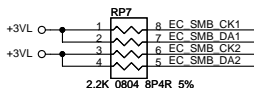
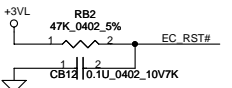
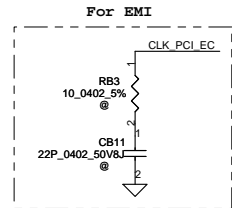
CardReader & Audio Conn.



TPM1.2 on board

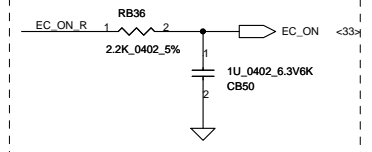


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev A
					4019IS	
				Date:	Monday, March 26, 2012	Sheet 26 of 40

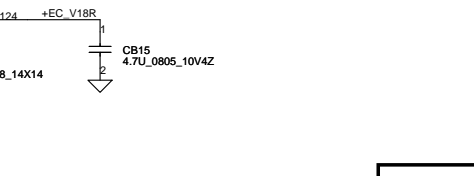
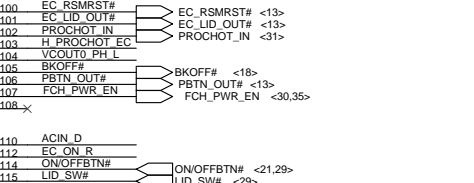
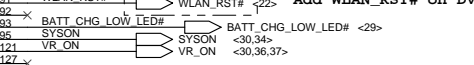
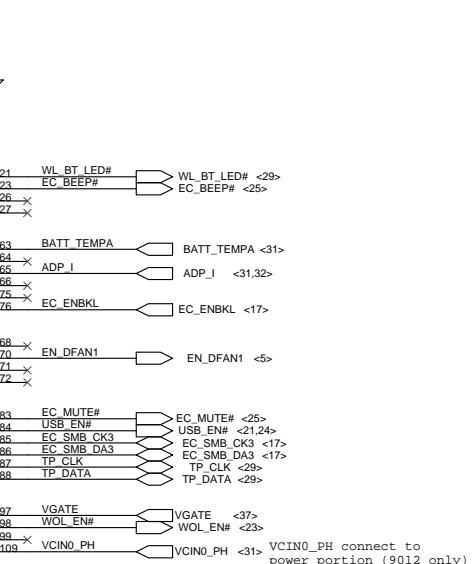


Voltage Comparator Pins FOR 9012 A3

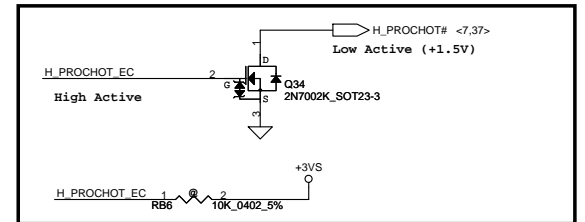
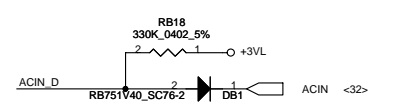
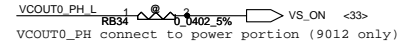
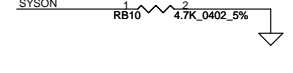
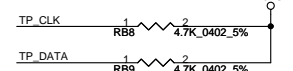
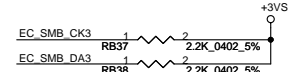
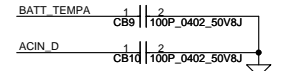
VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



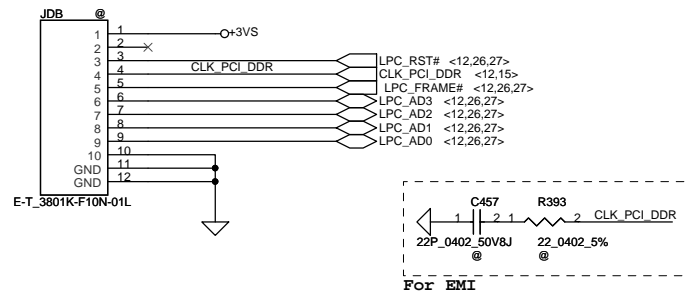
For KB9012 EC_ON low pulse work around



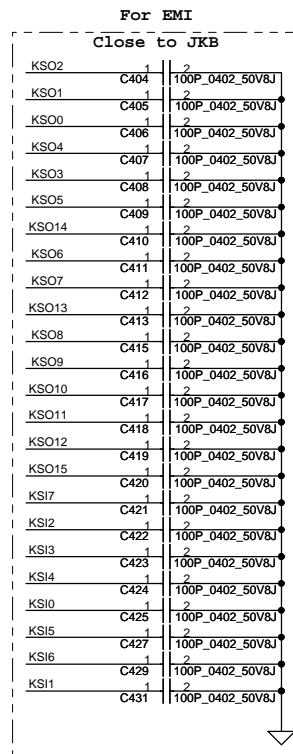
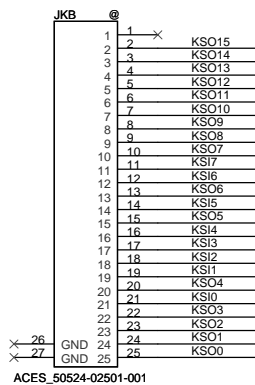
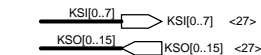
For KB9012 EC_ON low pulse work around



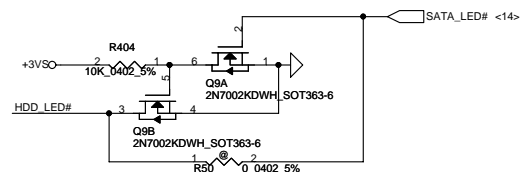
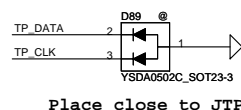
LPC Debug Port



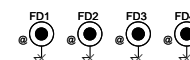
KEYBOARD CONN.



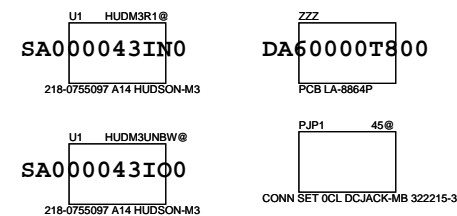
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					4019IS
Date:		Monday, March 26, 2012		Sheet	28 of 40



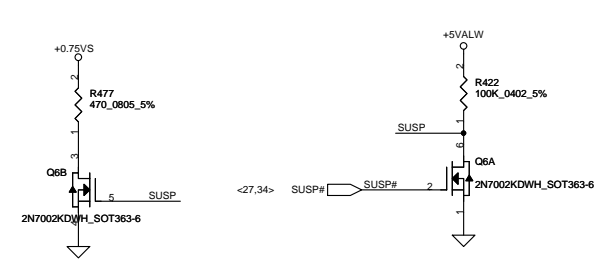
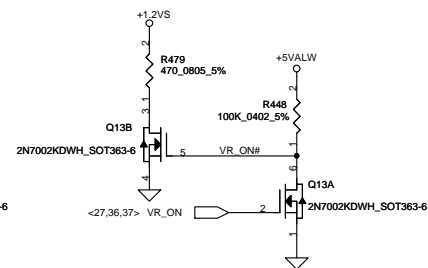
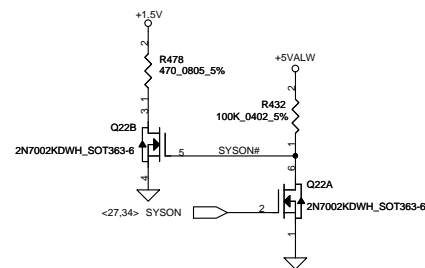
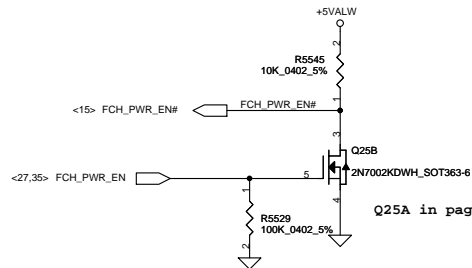
PCB Fedical Mark PAD



ISPD



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RA DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019IS	
				Date:	Monday, March 26, 2012	Sheet

[illegible][illegible]

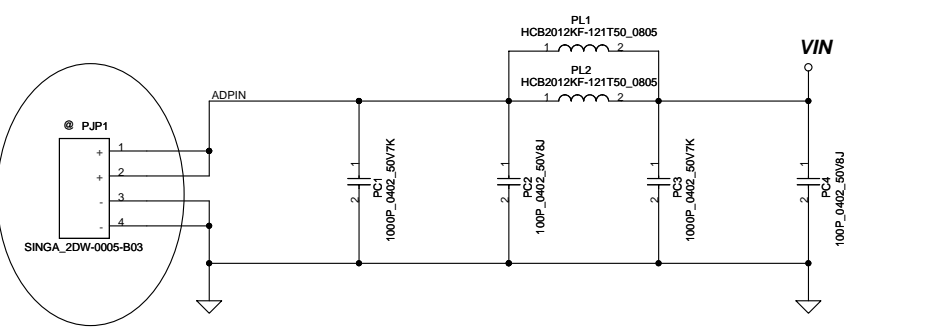
+5V_S TO +5V_S_ODD

The schematic diagram illustrates a driver circuit for converting a +5V_S signal to a +5V_S_ODD signal. The circuit consists of the following components and connections:

- Input Stage:** A +5V_S input signal is connected to a 470_0805_5% resistor (R457). The other end of R457 is connected to the gate of a 2N7002DMW SOT363-6 MOSFET (Q53B). The source of Q53B is connected to ground, and its drain is connected to the +5V_S signal.
- Driver Stage:** A +5V_ALW input signal is connected to a 100K_0402_5% resistor (R441). The other end of R441 is connected to the gate of a 2N7002DMW SOT363-6 MOSFET (Q53A). The source of Q53A is connected to ground, and its drain is connected to the +5V_S signal.
- Output Stage:** The +5V_S signal is connected to the gate of an AO3413_SOT23 MOSFET (Q45). The source of Q45 is connected to ground, and its drain is connected to the +5V_S signal. A 0.1U_0402_16V7K capacitor (C471) is connected between the gate and source of Q45. A 0.01U_0402_25V7K capacitor (C217) is connected between the gate and drain of Q45. A 4.7U_0805_10V4Z capacitor (C679) is connected between the gate and source of Q45. A 4.7V_0805_6.3V6K capacitor (C680) is connected between the gate and drain of Q45.
- Output Signal:** The +5V_S signal is connected to the gate of a PJP28 JUMP_43X79 MOSFET (PJP28). The source of PJP28 is connected to ground, and its drain is connected to the +5V_S signal. A 0.1U_0402_16V7K capacitor (C471) is connected between the gate and source of PJP28. A 0.01U_0402_25V7K capacitor (C217) is connected between the gate and drain of PJP28. A 4.7U_0805_10V4Z capacitor (C679) is connected between the gate and source of PJP28. A 4.7V_0805_6.3V6K capacitor (C680) is connected between the gate and drain of PJP28.

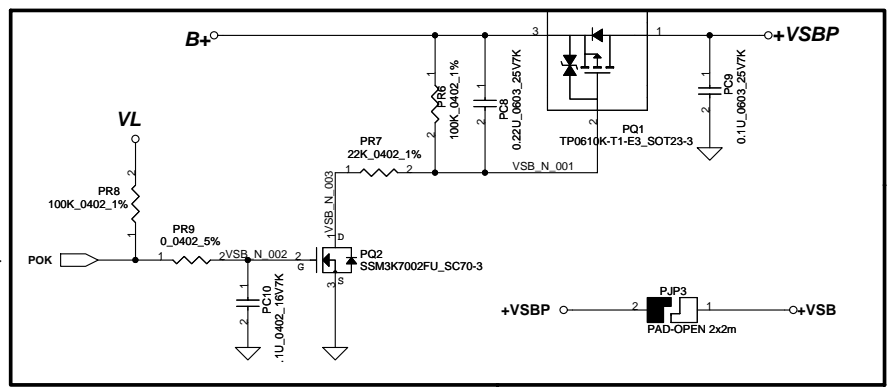
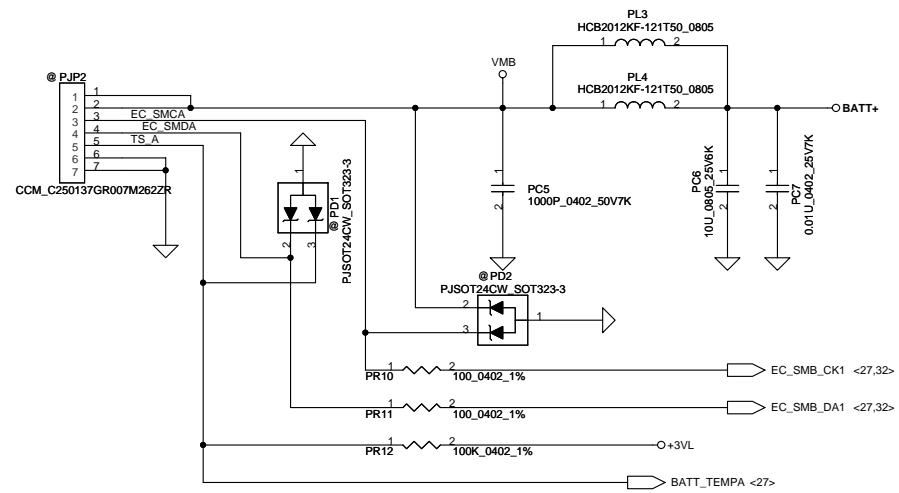
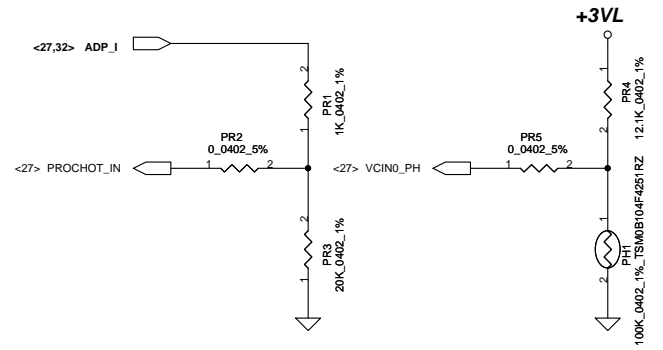
The circuit is labeled **+5V_S TO +5V_S_ODD**.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/21	Deciphered Date	2011/12/11	Title	SCHEMATIC, MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	4019IS
				Date:	Monday, March 26, 2012
				Sheet	30 of 40
				Rev	A

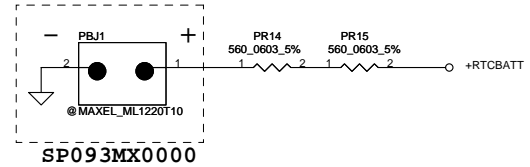


PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

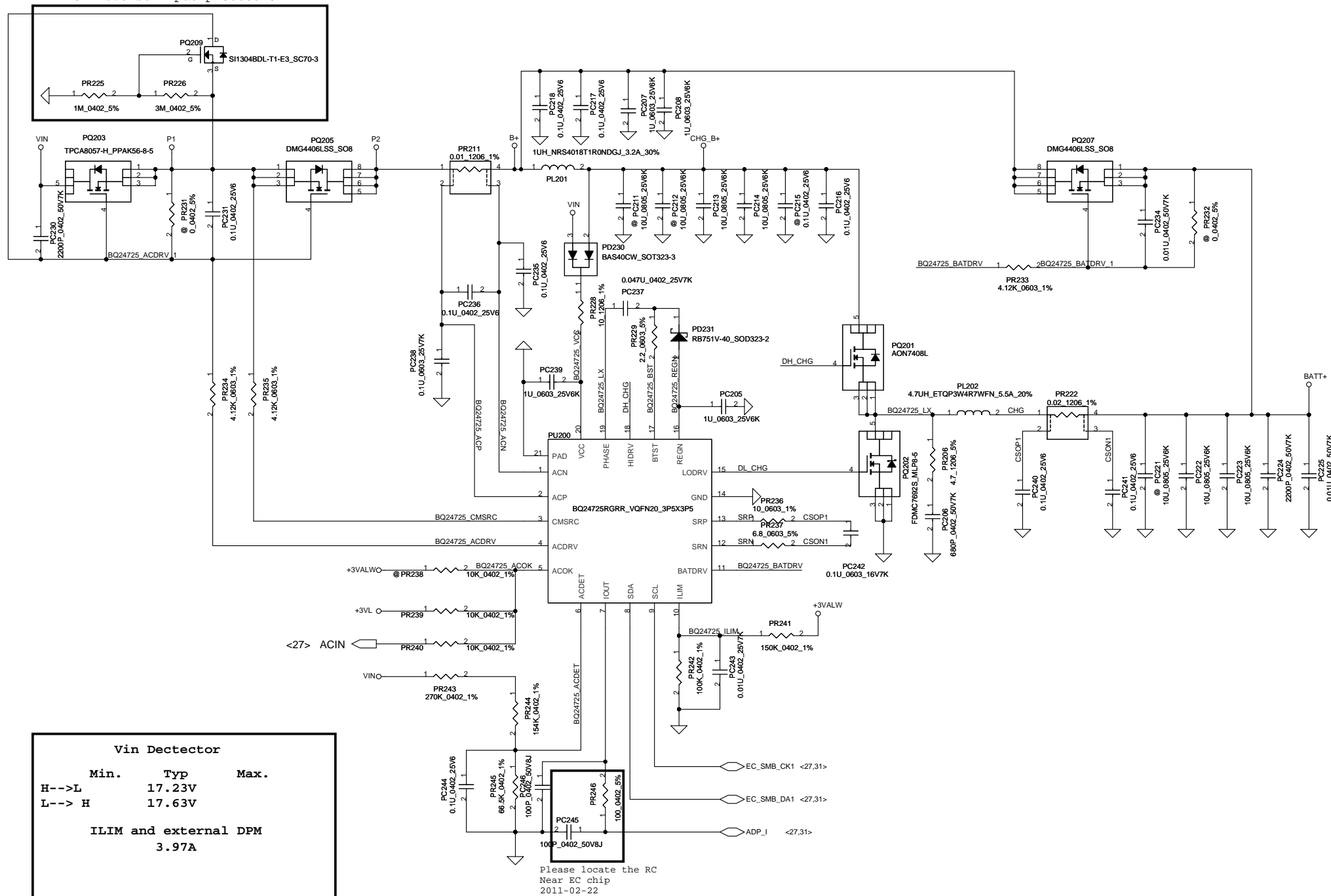
Please locate these parts
Near EC chip



RTC Battery

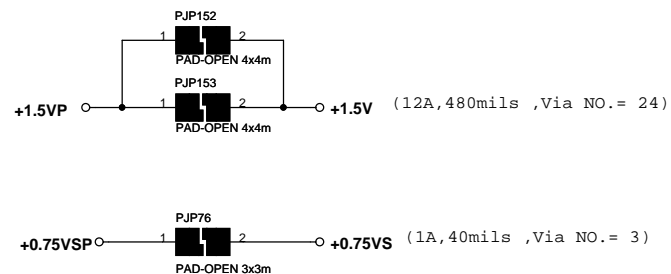


for reverse input protection

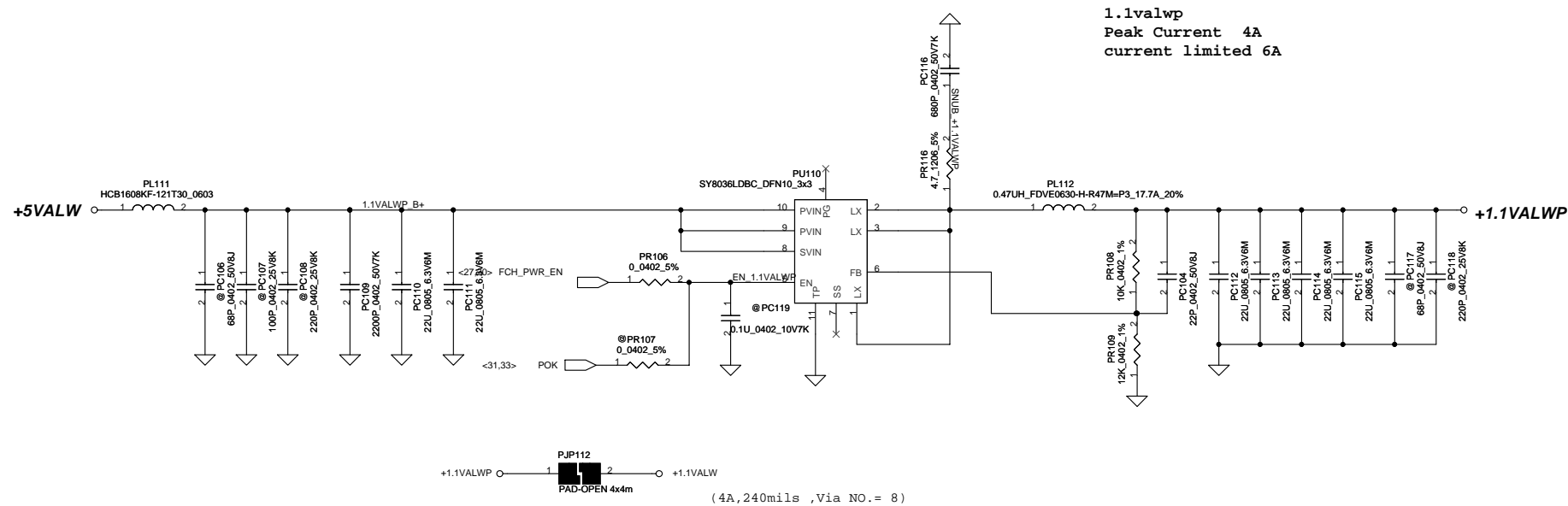


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

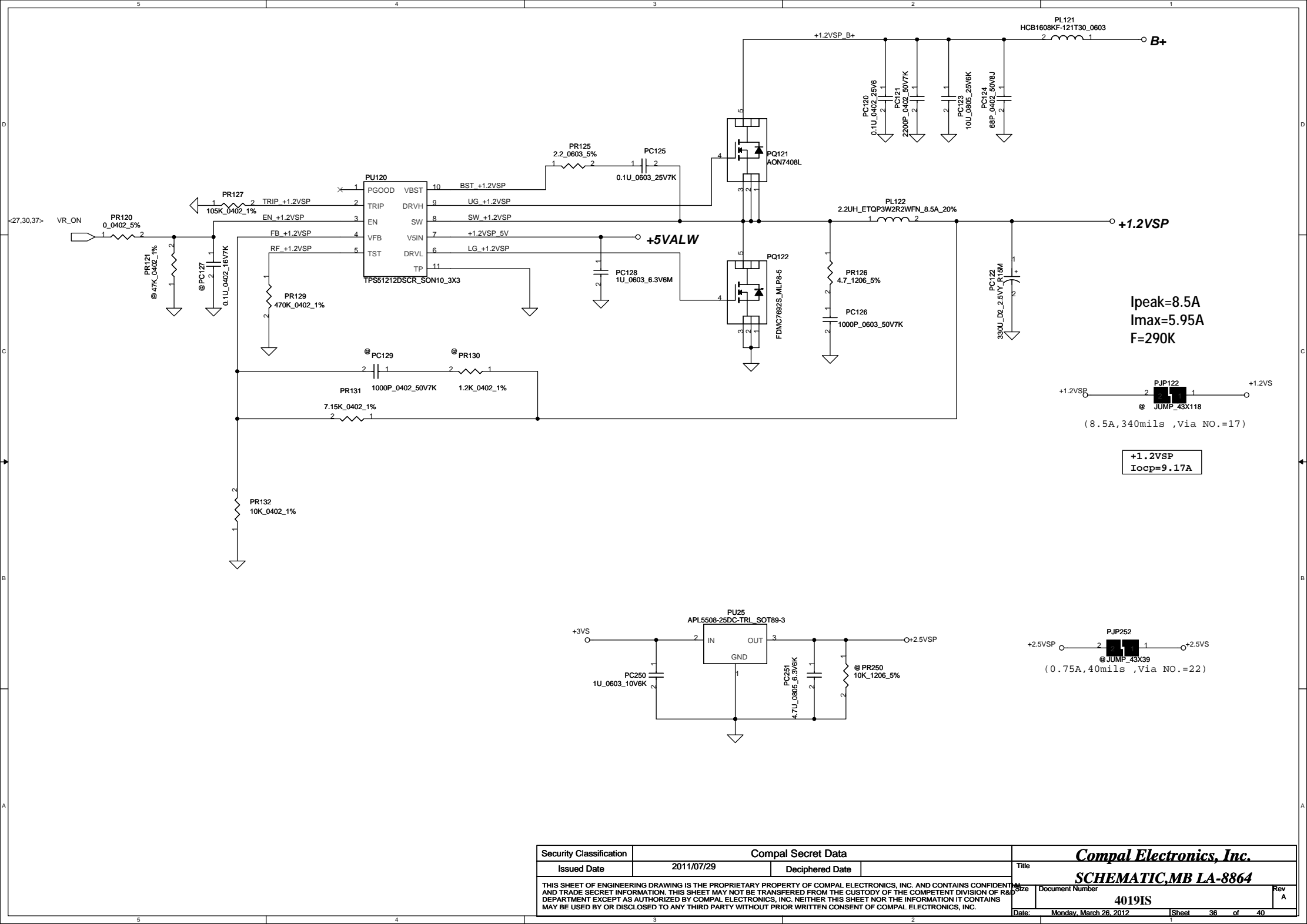
Note: S3 - sleep ; S5 - power off



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	SCHEMATIC,MB LA-8864
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019IS
				Date:	Monday, March 26, 2012
				Sheet	34 of 40

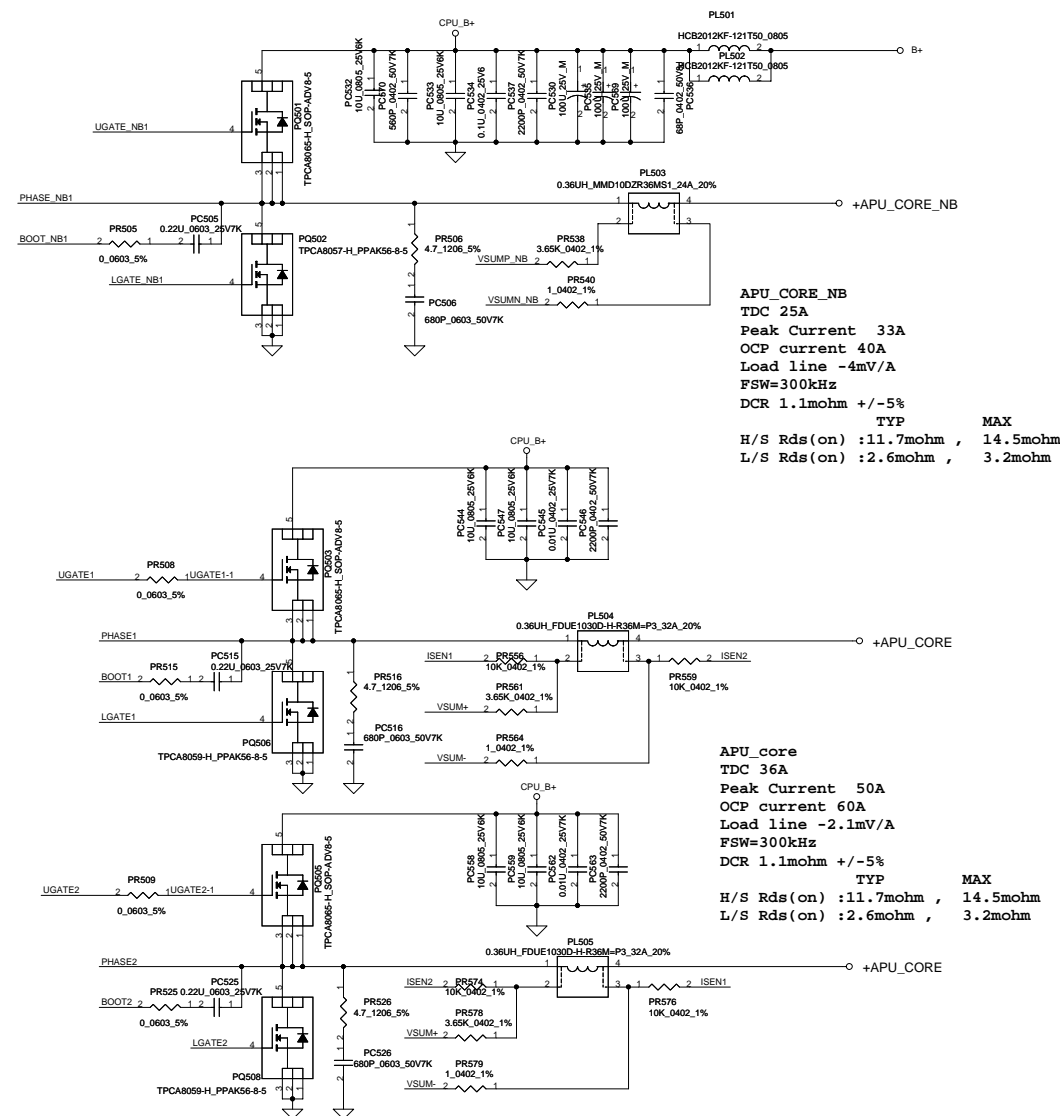


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/07/29	Deciphered Date		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				4019IS	A
				Date: Monday, March 26, 2012	Sheet 35 of 40



Security Classification		Compal Secret Data		Title	
Issued Date		2011/07/29		Deciphered Date	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Date		Monday, March 26, 2012	
Sheet		36		of 40	

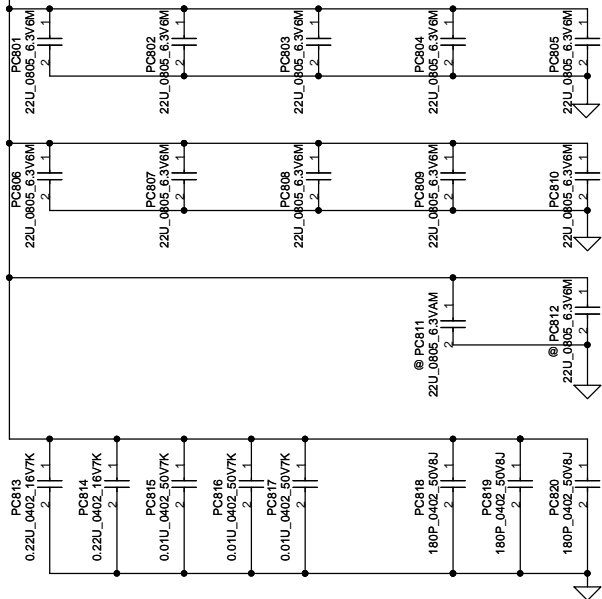
Compal Electronics, Inc.		SCHEMATIC, MB LA-8864	
4019IS		Rev A	



Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> SCHEMATIC, MB LA-8864		
Issued Date	2011/04/18	Deciphered Date	2015/07/08	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev A
					4019IS	
				Date:	Monday, March 26, 2012	Sheet 37 of 40

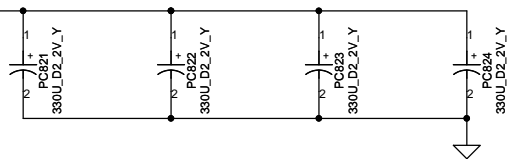
+APU_CORE

+APU_CORE



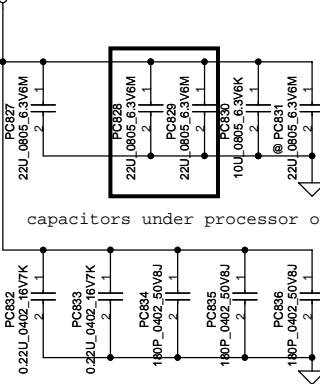
+APU_CORE

Local



+APU_CORE_NB

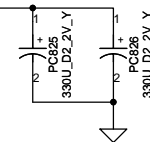
+APU_CORE_NB



capacitors under processor on bottom side of board

+APU_CORE_NB

Local



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/07/29		Deciphered Date	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Title		SCHEMATIC, MB LA-8864	
Size A3		Document Number		4019IS	
Date		Monday, March 26, 2012		Sheet 38 of 40	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/01/04	P31-PWR-DCIN/BATT CONN/OTP	Change PQ1 to SB906100280	Change source
2.	2012/01/04	P32-PWR-CHARGER	Change PQ209 to SB00000GC10,PQ203 to PCA8057 PQ202 to FDMC7692,PR241 to150K,PR243 to 270K Change PC211,PC212 to unmount ,add PC206,PR206	Change source Circuit modify
3.	2012/01/04	P33-PWR-3.3VALWP/5VALWP	Change PR350 to 30K,PR351 to 20K,PR337,PR357 to120K add PC336,PR336,PC356,PR356	Circuit modify
4.	2012/01/04	P34-PWR-1.5VP/+0.75VSP	Add PR156,PC156	
5.	2012/01/04	P37-PWR +CPU_CORE	Change PL503 to SH00000HD00,PQ502 to TPCA8057	Change source

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2012/12/31	SCHEMATIC,MB LA-8864	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				4019IS	A
Date: Monday, March 26, 2012				Sheet	39 of 40

HW PIR (Product Improve Record)

QMLE4 LA-8864P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/02/13

Item	Date	Page	Solution	Request
1.	1/10	P23	Add PJ31	For saving power consumption
2.	1/12	P29	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P25	Add internal MIC to MB	For customer request
4.	1/31	P23	Swap UL3 MDI0 and MDI1	For LAN trace routing
5.	2/1	P22	Add PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P26	Update JCRI0 pin definition	Change int. MIC to MB
7.	2/2	P25	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P22	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P27	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/8	P23	Add test point TL1 for pin37	For vendor request
11.	2/8	P29	Add screw H17, H20 and H21	For ME request
12.	2/9	P10	Change C218 from 390U to 330U (SF000002080)	For cost down
13.	2/9	P20	Reserve ESD D94~D96 for HDMI	For ESD request
14.	2/9	P19	Remove D3~D5 and add D97 and D98	For ESD request
15.	2/9	P23	Reserve ESD D99 and D100 for LAN	For ESD request
16.	2/9	P21	Add resistors to improve SATA signal quality	For SATA ODD co-layout
17.	2/10	P7	Stuff C126 and C127	For EMI request
18.	2/10	P22	Stuff CCL10	For EMI request
19.	2/10	P7	Reserve R77 and R85	For DeepS3 leakage
20.	2/21	P23	Change UL3 and UL4 PN to SP050006N00	For EMI request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121~R124,R118,R119	For debug use
5.	3/7	P27	Update UL3 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20,RB34,R3,RV102,R425,R136,R31,R32,R33,RV284,RV287 R62,RV277 to short pad	
8.	3/12	P20	Add C201 and C214	For EMI request
9.	3/12	P21	Add C364 and C365	For EMI request
10.	3/12	P25	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process

www.s-manuals.com